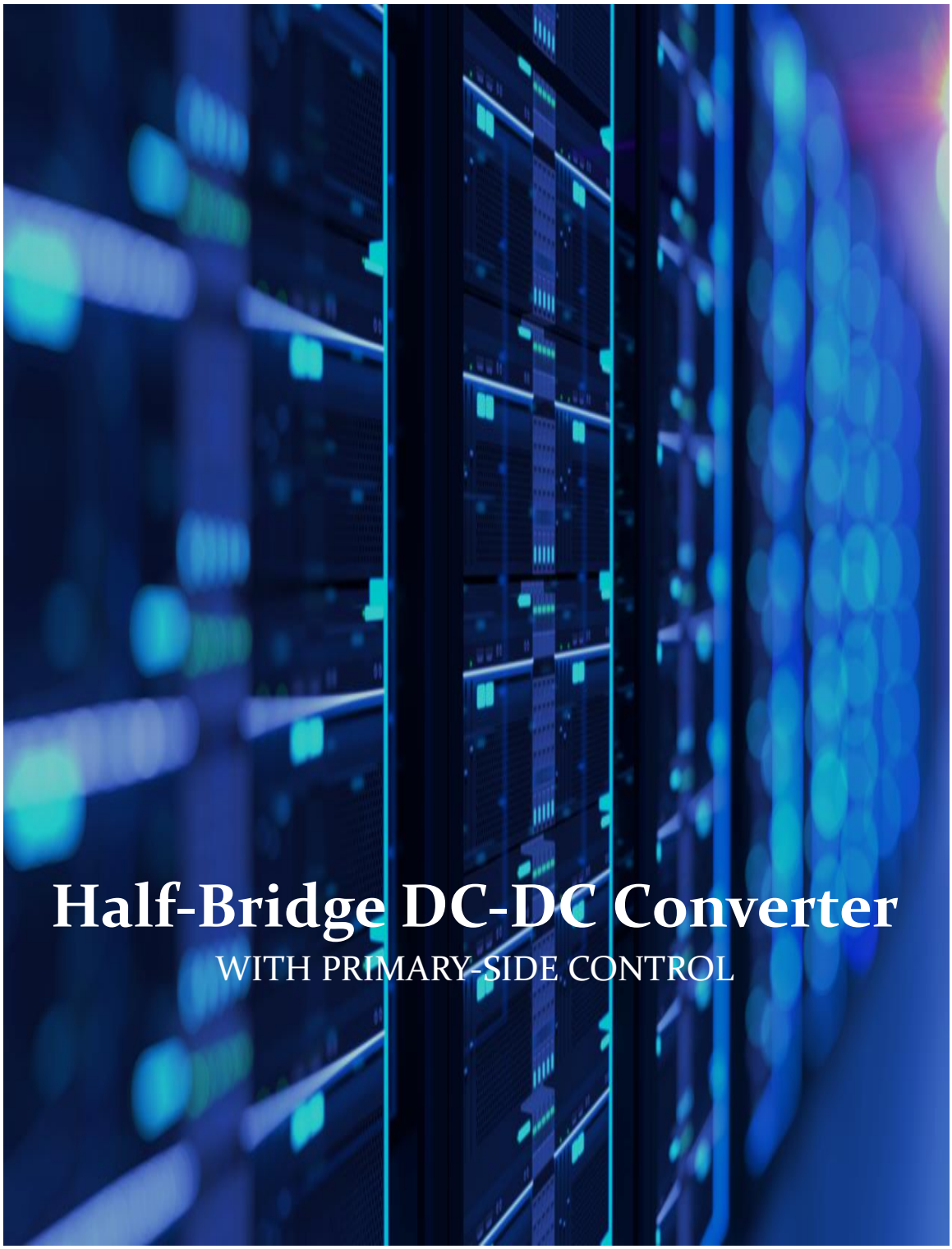


Half-Bridge DC-DC Converter

WITH PRIMARY-SIDE CONTROL

1 Introduction to Half-Bridge DC-DC converters

A half-bridge converter is a type of DC-DC converter that can supply an output voltage either higher or lower than the input voltage and can provide electrical isolation via a transformer. In comparison to a flyback or forward converter, the half-bridge converter design can yield higher output power and use parts that are smaller and less expensive[8]. The double-ended topology of the half-bridge converter helps to maximize the utilization of the transformer. The other popular double-ended topologies are push-pull and full-bridge.

1.1 TYPICAL APPLICATIONS

These half-bridge converters are well suited for applications requiring high conversion efficiency with wide input voltage variations and those which require low voltage and high current output. Some applications include Telecom power supplies, Server systems, DC microgrid and ASIC's.

1.2 SCOPE OF THIS DESIGN EXAMPLE

The example uses a UCC28250 PWM controller from TI to realize a DC-DC symmetrical half-bridge topology with primary-side control that converts 36V to 72V DC to a regulated output voltage of 3.3 V with 23A maximum load current. The design is based on the EVM from TI using UCC28250. The nominal input voltage is 48V. The controller UCC28250 is modeled using the MAST language in SaberRD.

FEATURES:

- Output voltage regulation from no load to full load.
- Control driven synchronous rectifier.
- Voltage mode control.
- Non-latching input over voltage protection.
- Hiccup over current protection.

2 Half-bridge DC-DC Converter with primary-side control - Schematic in SaberRD

The schematic of the DC-DC Converter realized using UCC28250 is as shown in Figure 1 below.

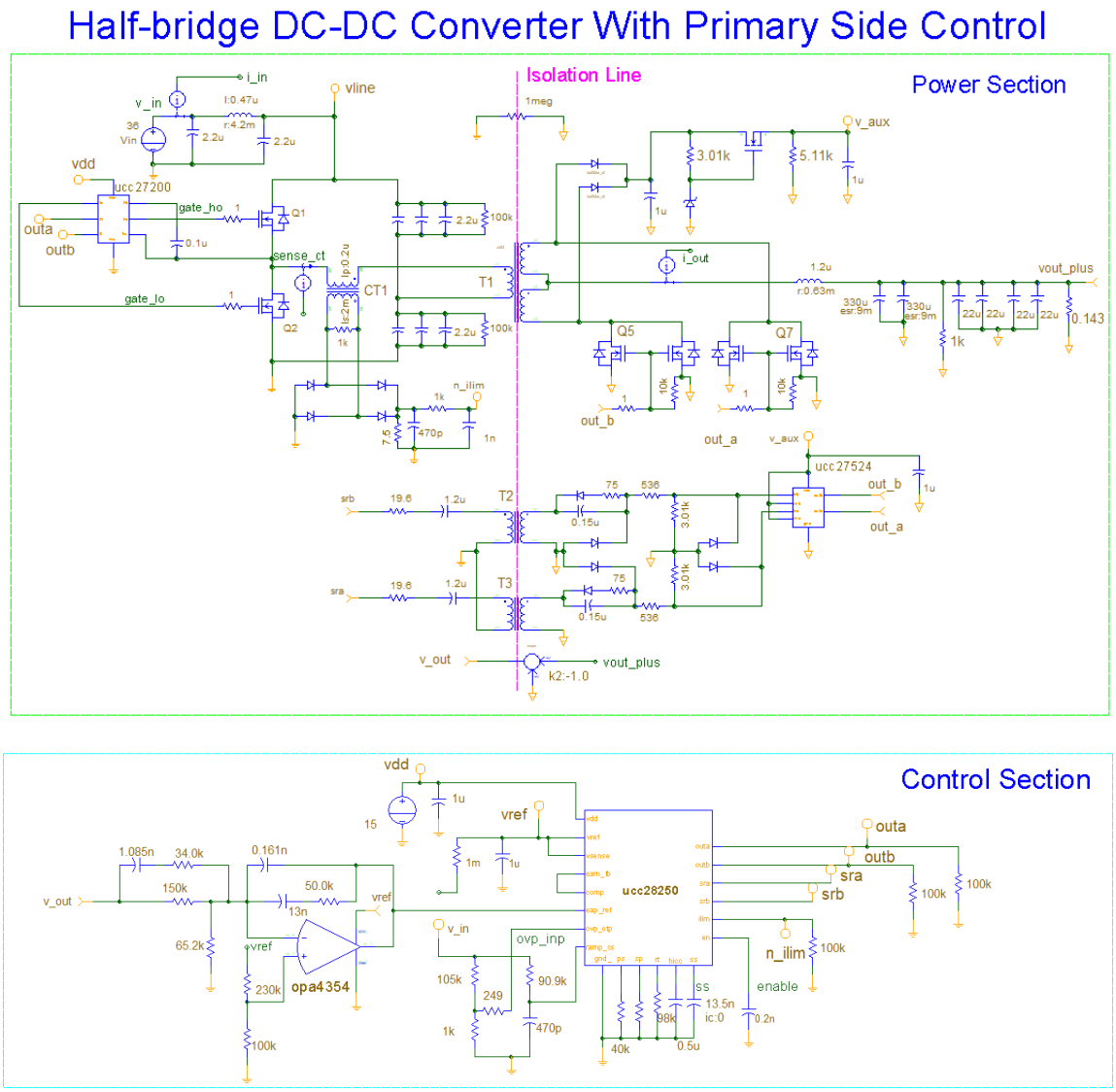


Figure 1: Schematic of Half-bridge DC-DC Converter with primary-side control using UCC28250

2.1 DESIGN SPECIFICATIONS AND BOUNDARY CONDITIONS

The below Table 1 shows the nominal design specifications for the design.

NOMINAL SPECIFICATIONS		
Name	Symbol	Value
Input Voltage	Vin	36V to 72V
Output Voltage	Vout	3.3V
Max Output Power	Pout max	75W
Switching Frequency	Fsw	150kHz
Max. Ripple Voltage on Vout	ΔVout	50mV
Pk-Pk Output Inductor Ripple Current	ΔIL	6.90A
Output current	Iout	23A
Efficiency at Full load	η	90%

Table 1: Specification for typical input values

3 Operation of half-bridge DC -DC converter

Figure 2 shows a power stage diagram of a Half-Bridge topology power converter. There are three operational states for a Half-Bridge power converter. These are explained in reference [4]. The transformer secondary is arranged in a center tapped configuration with the center tap connected to the output LC filter.

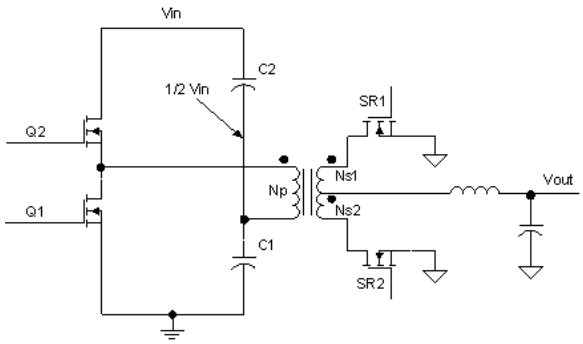


Figure 2: Power stage diagram of a Half-Bridge topology

Synchronous rectifiers are used for secondary rectification. With half-bridge converters, the synchronous MOSFETs are normally turned on. However, when one of the primary MOSFETs is turned on, the synchronous MOSFETs are turned off.

3.1 PREBIAS AND SOFT-START

Prebias is defined as a voltage that is present at the output of the converter before the converter is switched on. This prebias can be present for several reasons. The issue with a prebias is that if any converter has synchronous rectification, it would be possible to discharge the output during startup. It is necessary for the output voltage to charge to its required regulation voltage and not to go through any discharge of the output if a prebias exists prior to startup[3]. The controller

UCC28250 has a dedicated internal prebiased start-up control loop that works in conjunction with a primary-side voltage loop, which achieves prebiased start-up for either primary-side or secondary-side control applications[1].

Soft-start is a feature that prevents component stresses during startup of the converter. In addition, it limits the inrush current at startup and allows a monotonic voltage startup [3]. The controller UCC28250 has a programmable soft-start and Hiccup restart timer feature[1].

4 Choosing the components for the Design Specification

4.1 CHOOSING A CONTROLLER MODEL

In this design example, an advanced PWM controller UCC28250 from TI is used to realize a half-bridge topology as discussed above. The integrated synchronous rectifier controls outputs in this controller help to achieve high efficiency and high-performance topologies, including half-bridge, full-bridge, interleaved forward, and pushpull[1].

4.1.1 SABER COMPONENT MODEL FOR UCC28250

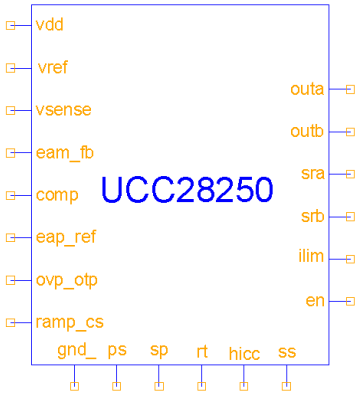
The Saber Component model for UCC28250 is designed based on the functional block diagram given in the datasheet [1]. The component functions are divided into blocks and implemented in the model.

- Oscillator Frequency And Dead Times Programming
- Undervoltage Lockout, Enable And Soft-start
- Vdd And Reference Voltage Output
- Ramp Generation
- Overvoltage / Overtemperature And Cycle By Cycle
- Overcurrent Protection With Hiccup Mode
- Primary Gate Signals And Synchronous Rectifier Gate Signals Generation
- Prebias Start-Up Section

MODEL LIMITATIONS

- Thermal effects are not included.
- Supply currents may slightly differ than the datasheet specification (section 6.5) [1].
- Prebiased start-up section might need additional refinement as sufficient details are not given in the datasheet.

SABER MODEL AND PIN MAPPING



Pin No	Datasheet Pin Name	Saber Symbol Pin Name
1	VSENSE	vsense
2	RT	rt
3	RAMP/CS	ramp_cs
4	ILIM	ilim
5	EN	en
6	OVP/OTP	ovp_otp
7	VREF	vref
8	REF/EA+	eap_ref
9	FB/EA-	eam_fb
10	COMP	comp
11	SS	ss
12	SP	sp
13	PS	ps
14	HICC	hicc
15	OUTA	outa
16	OUTB	outb
17	SRA	sra
18	SRB	srb
19	VDD	vdd
20	GND	gnd_

Table 2: Pin-Mapping of UCC28250 Saber Model

4.1.2 NEED FOR ADDITONAL MOSFET DRIVERS IN DESIGN

OUTA and OUTB are the primary-side switch control signals whereas SRA and SRB are the synchronous rectifier control signals with a 0.2-A peak current capability. Hence, an external gate driver is required [1].

The UCC27200 half-bridge driver and UCC27524 MOSFET driver are used in conjunction with the UCC28250 to provide a complete power converter solution. The spice models provided by TI for these MOSFET Drivers were translated to Saber by using the Spice-to-Saber Translator before been used in this design.

Note: These driver models can also be built in Saber using generic building block models available in the Saber library. Or else, by using the MAST modeling language.

4.2 CHOOSING A SWITCHING FREQUENCY

For this design, we choose oscillator frequency, Fosc as 300 kHz. Each output switch operates at half the oscillator frequency. Switching frequency, Fsw = ½ x Fosc=150kHz. OUTA, OUTB, SRA, and SRB are the output switch signals from the controller UCC28250.

The dead time $T_{D(sp)}$ between the synchronous rectifier turnoff and primary output turnon can be programmed by an external resistor, R_{SP}, connected between the SP pin and ground. The dead time $T_{D(ps)}$ between the primary output turnoff and synchronous rectifier turnon can be set by an external resistor, R_{PS}, connected between the PS pin and ground. Zero dead time can be achieved by tying the SP pin and PS pin to VREF[1].

In this design we used 65ns for dead time $T_{D(sp)}$ and $T_{D(ps)}$. This is set by choosing 40kΩ for R_{SP} and R_{PS}.

The oscillator frequency is set to 300kHz by connecting an external resistor RT=98kΩ between pin RT and ground as calculated from datasheet [1].

4.3 CALCULATING THE RAMP GENRATION, SOFT-START, CURRENT LIMIT, OVER VOLTAGE PROTECTION COMPONENTS FOR UCC28250

The UCC28250 can be controlled using either voltage mode or current mode. RAMP/CS is a multi-function pin used either to generate the ramp signal for voltage mode control or to sense current for current mode control. In this example, we use Voltage mode control. The Rcs=90.9kΩ and Ccs=470pF values are calculated according to the equations in the datasheet to generate a 300kHz pulse. The generated ramp signal is used by the controller to control the duty cycle for both the primary-side switches and secondary-side synchronous rectifiers.

To achieve the input voltage feedforward, Rcs is tied to the input line voltage. This provides a much better line transient response for the converter. The input voltage feedforward also helps with the prebiased start-up.

The SS pin used to program Soft-start is connected to Css=13.5nF. A small value of Css is used here to achieve Tss of ~1.6ms to speed up the operation of converter to save the simulation time. To increase the Soft-start time, a higher Css value can be calculated and used.

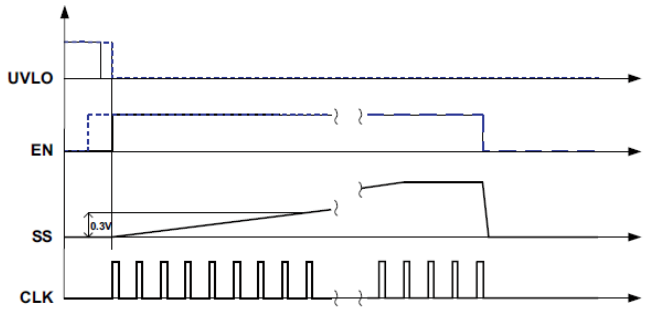


Figure 3: Level Enable at EN pin

Cycle-by-cycle current limit is accomplished using the ILIM pin for both the current mode control and voltage mode control. The input to the ILIM pin represents the primary current information. If the voltage sensed at ILIM pin exceeds 0.5V, the current sense comparator terminates the pulse of output OUTA or OUTB.

Over current protection level, Ipk is calculated as below.

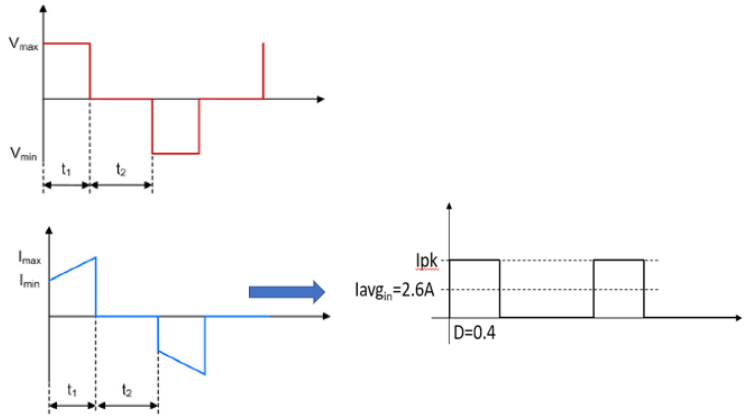


Figure 4: Half-Bridge – Primary side Voltage and current waveforms for CCM

- The max input current allowed is 2.35A (at Vin=36V and Iload=23A)[2].
- The average input current approximated as Iavgin=1/10*Iout=2.6A
- (at output over current, Iload=26[2]).
- Duty at 36V is approximately D=0.4.
- Input current waveform assumed as rectangular. Iavgin=Ipk*D.
- Ipk = 2.6A/0.4=6.6A.

The ILIM resistor and capacitor Rs=7.5Ω and Cs=470pF are calculated as per the datasheet by using the Ipk from above, and RC constant of filter as 3.5ns.

The cycle-by-cycle current limit operation time before all four outputs are shutdown is programmed by external capacitor Chicc. In this example, we use Chicc=0.5uF by assuming off time, Toc=4ms.

If the voltage on the OVP/OTP pin exceeds 0.7 V, a fault shutdown occurs. Input over voltage threshold is 73V. Accordingly, the over voltage protection resistors are chosen as R1=105kΩ, R2=1kΩ and R3=249Ω after the calculation as per the datasheet.

4.4 CHOOSING THE TRANSFORMER AND CALCULATION OF THE SWITCHING DUTY CYCLE-D

The transformer chosen here is DA2025-AL from Coilcraft with turns ratio Np/Ns as 8T/2T.

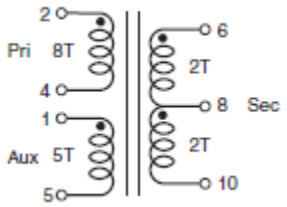


Figure 5: Transformer T1 -DA2025-AL winding ratio from datasheet

The frequency of the switching input MOSFET in a half-bridge converter is half the oscillator frequency. The duty cycle of OUTA or OUTB can be calculated as per the below equation at 72-V input voltage (Vin) and 3.3V output (Vout).

$$D = \frac{n * Vout}{Vin/2} * 1/2$$

Where n is the transformer turns ratio (Np/Ns).

$$D = \frac{4 * 3.3}{72/2} * 1/2 = 0.183$$

Duty cycle of SRA or SRB can be calculated as below.

$$SR\_D = 1 - D = 1 - 0.183 = 0.816$$

4.5 DESIGNING VOLTAGE FEEDBACK LOOP

An Op-Amp OPA4354 from TI is selected for error amplification. An Op-Amp requires local feedback (between its output and inputs) to make it stable. A Type I compensator was designed and tested. With the Type I compensator, it is found that the control loop is unstable, and the required output was not achieved at the given frequency through simulation. The purpose of adding compensation to the error amplifier is to counteract some of the gains and phases contained in the control-to-output transfer function that could jeopardize the stability of the power supply.

A Type II compensation scheme adds an RC branch to flatten the gain and improve the phase response in the mid-frequency range. Type II compensators are usually reserved for current-mode control compensation because it cannot be used to improve the phase of the power stage.

A Type III compensation scheme adds another RC branch to the Type II compensator and is the one used to compensate voltage-mode converters operating in CCM [6]. In this design a Type I compensator was replaced with a Type III compensator.

Reference voltage for error amplifier is set to 1V (a voltage divider of 230kΩ and 100kΩ is used) and output voltage required is, Vout=3.3V.

$$\frac{Vout * rfb2}{rfb1 + rfb2} = 1V$$

$$\frac{rfb1}{rfb1 + rfb2} = 0.303$$

The component values for rfb1, rfb2, rfb3, rfb4, cfb3, cfb4, and cfb5 for the Type III compensation circuit are calculated and adjusted from simulation to stabilize the control loop for the given input voltage range and frequency [6].

4.6 CALCULATING THE OUTPUT INDUCTOR

The average current IL_{avg} that flows through the boost inductor is 23A. The maximum allowed ripple current, ΔIL =6.9A with continuous mode operation. The calculation of output Buck inductor is as below [7].

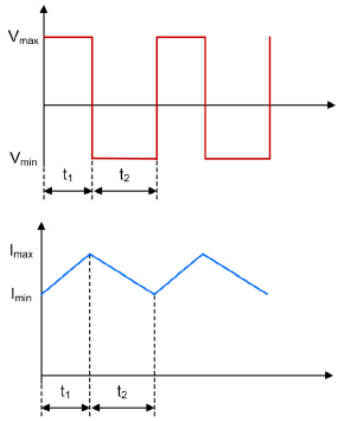


Figure 6: Half-Bridge - Inductor L1 Voltage and current waveforms for CCM

$$V_L = L\frac{di}{dt}$$

$$V_{Lmax} = \frac{1}{2} * Vin * \frac{Ns}{Np} - Vf_{sr} - Vout = \frac{1}{2} * 72 * \frac{2}{8} - 0.2 - 3.3 = 5.2V$$

$$L \cong \frac{V_L}{\Delta IL} * \Delta T = \frac{V_L}{\Delta IL} * \frac{D}{Fsw} = \frac{5.2V}{6.9A} * \left(\frac{0.183}{150k}\right) \geq 0.827\mu H$$

where ΔT is the off time of secondary synchronous MOSFET.

Time period =T= 1/150kHz = 6us.

Duty cycle SR_D = 0.816, D=1-SR_D=0.183.

An optimal value of 1.2uH is chosen for the Buck inductor to account for worst case conditions.

4.7 CALCULATING THE OUTPUT CAPACITOR

Half-Bridge output capacitor Cout, Voltage and current waveforms for continuous conduction mode, CCM are as shown below.

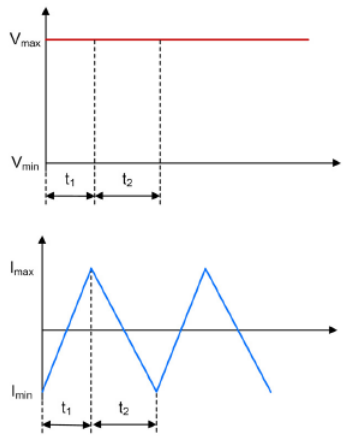


Figure 7: Half-Bridge - capacitor Co, Voltage and current waveforms for CCM

When the secondary MOSFET is ON, the output capacitor Cout must supply the load. Here Fsw=150kHz, ripple current allowed is 6.9A and voltage ripple allowed is 50mV. The Cout required and the maximum ESR allowed here is calculated as below.

$$ESR_{max} \cong \frac{\Delta \text{Vout}}{\Delta I_L} = \frac{50mV}{6.9A} = 7.24m\Omega$$

$$I_c = C * \frac{dv}{dt}$$

$$C \cong \frac{\Delta \text{T} * \text{Ic}}{\Delta V}$$

$$Cout\sim \geq \frac{\Delta I_L}{8 * \text{Fsw} * \Delta \text{Vout}} \geq \frac{6.9A}{8 * 50mV * 150kHz} \geq 115uF$$

A rule of thumb when selecting capacitance is to choose a value that is at least 20% higher than the minimum calculated capacitance, to account for capacitor tolerance.

4.8 SWITCHING MOSFET CONSIDERATIONS

An N-channel MOSFET RJK1053DPB from Renesas is used for primary switches with 4.5V gate drive compatibility. The breakdown voltage is 100V with sufficient margin (design rated max voltage at drain pin is 72V) and rated drain current of 25A (design rated input current is 2.35A).

RJK0453DPB N-channel Power switching MOSFET from Renesas is selected for secondary side switching in this design. It has a capability of 4.5V gate drive and drain current rating of 55A (design rated max current is 26A) and a breakdown voltage of 40V (design output voltage is 3.3V).

These MOSFET models are characterized by using the datasheet information in the Power MOSFET tool from SaberRD and are optimized for best accuracy..

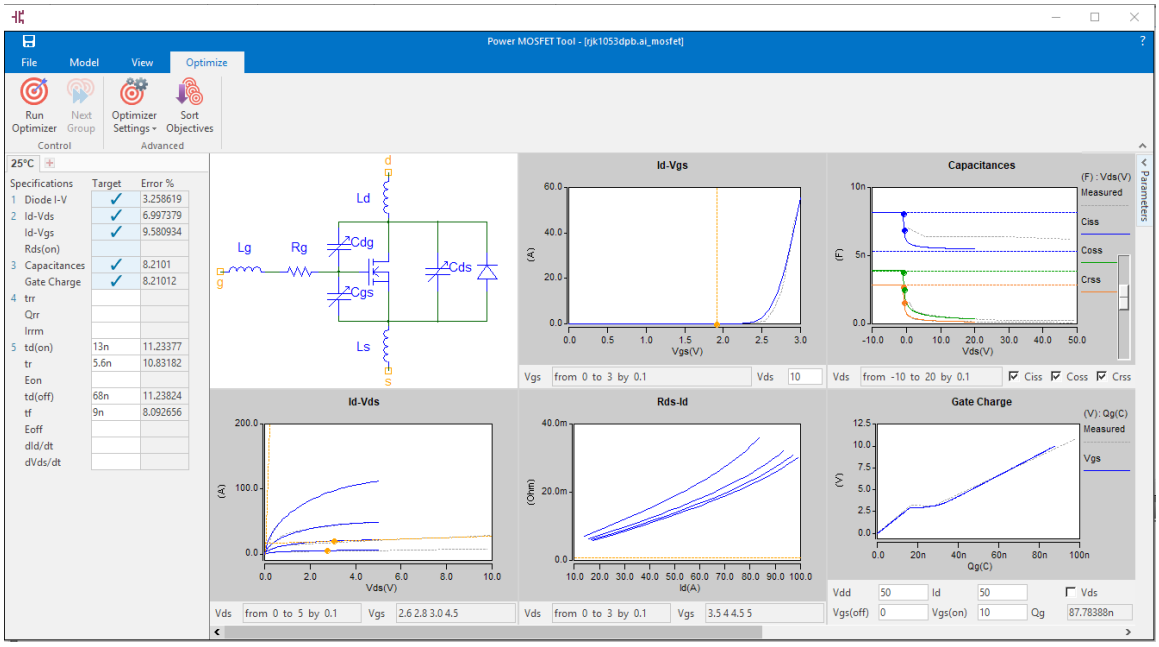


Figure 8: MOSFET model characterization for RJK1053DPB

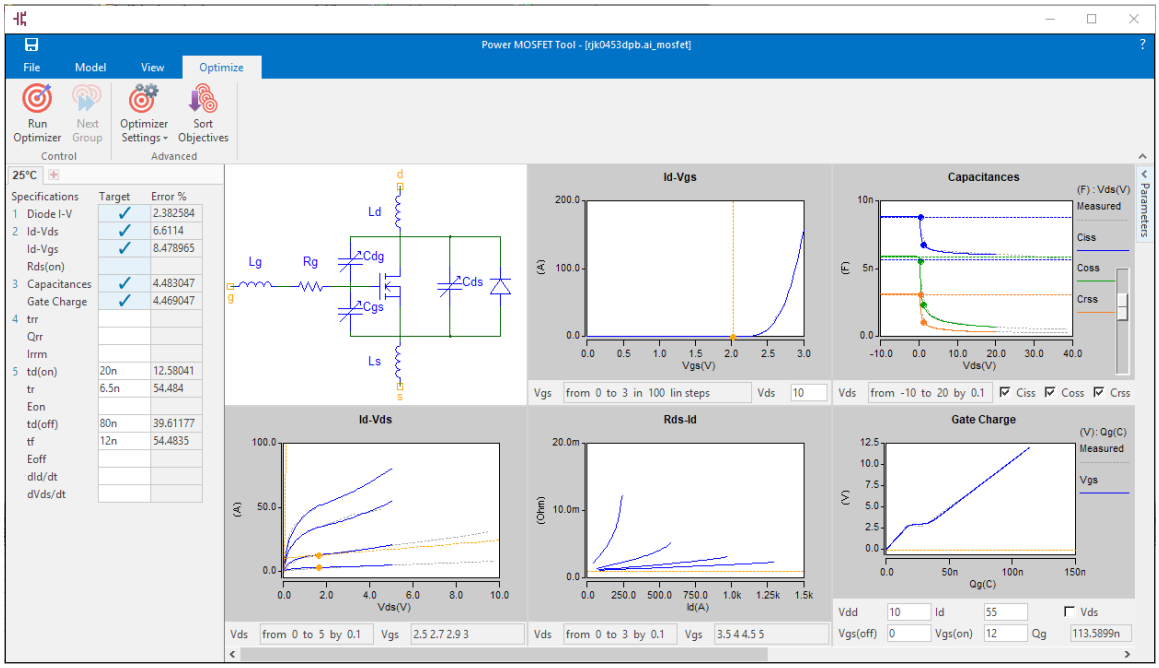


Figure 9: MOSFET model characterization for RJK0453DPB

Note:

1) The switching MOSFETS can be characterized further for other temperatures from datasheet and optimized to use in temperature vary analysis.

2) The tolerances and stress parameters can be included for Robust design analysis.

3) Also, a thermal model can be characterized to perform thermal analysis on the switching MOSFETs.

5 Simulation and validation in SaberRD

The design is simulated over time for nominal conditions using 36V and varied input voltages and the results are analyzed. Next, a fault simulation is done with the load shorted and with input over voltage condition. The following sections show the results and summary of these analyses. The experiments are created for these analyses in SaberRD to automate the tests and to report the results are as shown below.

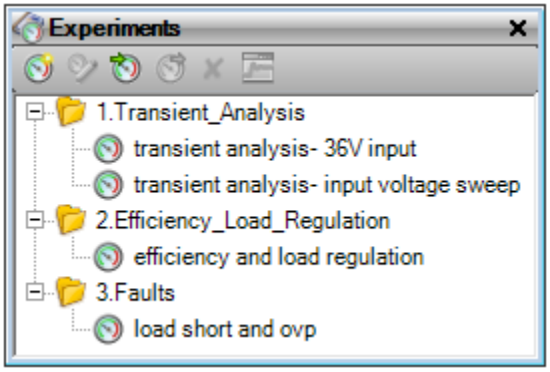


Figure 10: Experiments

5.1 PERFORMANCE DATA AND TYPICAL CHARACTERISTIC CURVES

Open the design `half_bridge_dc_dc_converter_v1` and run the experiments under the category `Transient_Anlaysis`. The experiment, `transient analysis- 36V input` runs a time-domain analysis with input voltage of 36V. The experiment `transient analysis- input voltage sweep` runs a time-domain analysis with varied input voltage.

5.1.1 EXPERIMENT TO RUN TRANSIENT ANALYSIS FOR INPUT VOLTAGE OF 36V AND OUTPUT LOAD CURRENT OF 23A

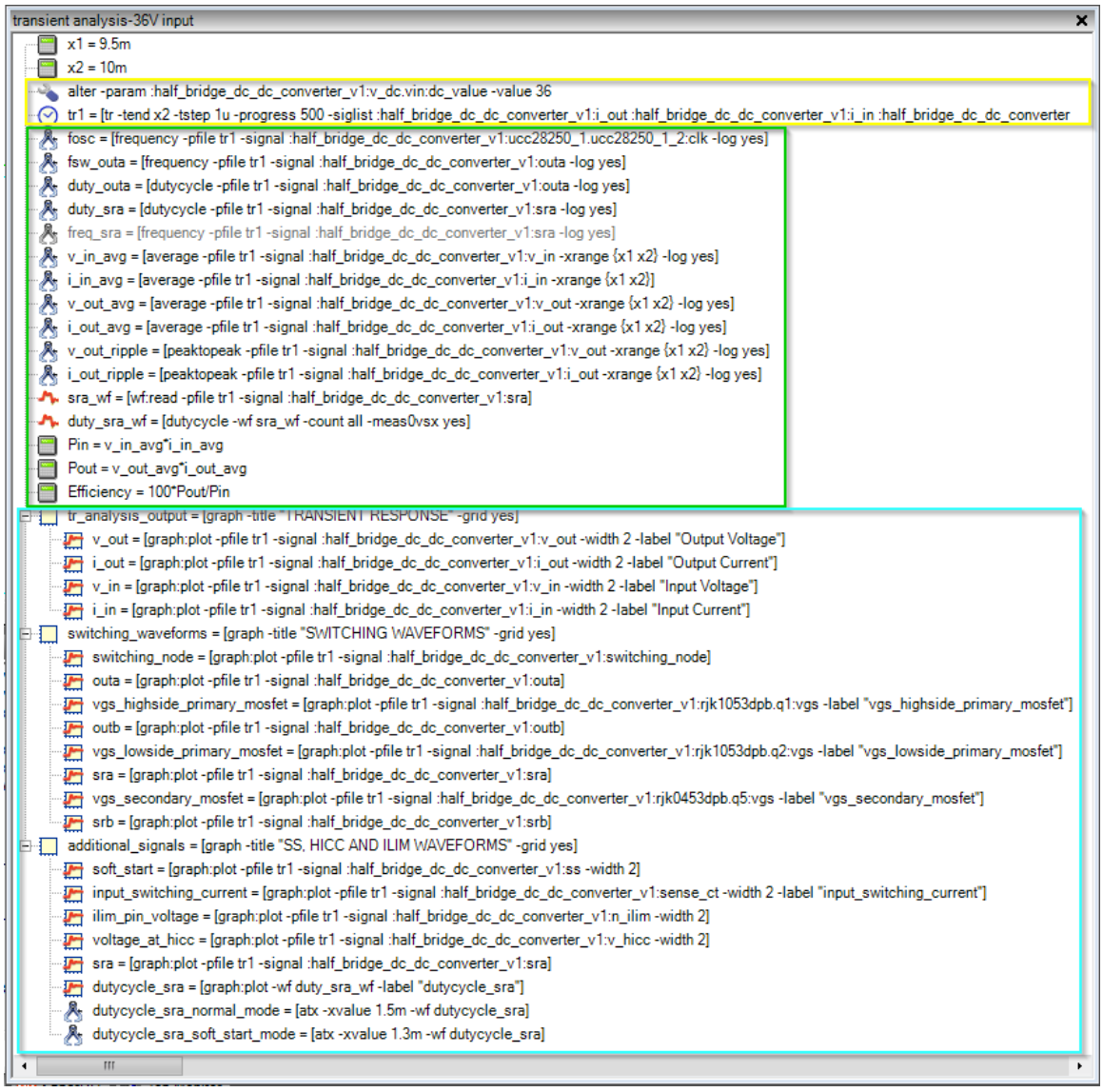


Figure 11: Experiment for time-domain analysis- 'transient analysis – 36V input'

Figure 11 shows the experiment, `transient analysis – 36V input` created in SaberRD to run a transient analysis and fetch the required results automatically after the analysis. The yellow highlighted part shows the transient analysis settings. The green highlighted part shows the measurements made on the results to be logged in the Experiment report. The blue highlighted part shows the Graphs created and the signals added to each graph.

5.1.2 TRANSIENT RESPONSE RESULTS FOR INPUT VOLTAGE OF 36V AND OUTPUT LOAD CURRENT OF 23A

transient_analysis_36V_input.ai_exptlog

Task Label	Task Definition	D	Task Result	Task Stat
fosc	fosc = [frequency -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:ucc28250.ucc28250_1:clk -log yes]		301322.77668313	Complete
fsw_outa	fsw_outa = [frequency -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:outa -log yes]		150661.31930258	Complete
duty_outa	duty_outa = [dutycycle -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:outa -log yes]		0.37242338976302	Complete
duty_sra	duty_sra = [dutycycle -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:sra -log yes]		0.61011977456925	Complete
v_in_avg	v_in_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_in -xrange {x1 x2} -log yes]		36.0	Complete
v_out_avg	v_out_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_out -xrange {x1 x2} -log yes]		3.300712212849	Complete
i_out_avg	i_out_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:i_out -xrange {x1 x2} -log yes]		23.085305392181	Complete
v_out_ripple	v_out_ripple = [peaktopeak -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_out -xrange {x1 x2} -log yes]		0.0064342479790...	Complete
i_out_ripple	i_out_ripple = [peaktopeak -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:i_out -xrange {x1 x2} -log yes]		2.221402888701	Complete
Pin	Pin = v_in_avg*i_in_avg		80.141095445058	Complete
Pout	Pout = v_out_avg*i_out_avg		76.197949445321	Complete
Efficiency	Efficiency = 100*Pout/Pin		95.079745319378	Complete

Figure 12: Experiment report from –'transient analysis – 36V input'

From the report above, we could see that the output voltage, Vout =3.3V is reached and stabilized before 10ms. The efficiency is 95%. Below are the Graph results from the Experiment.

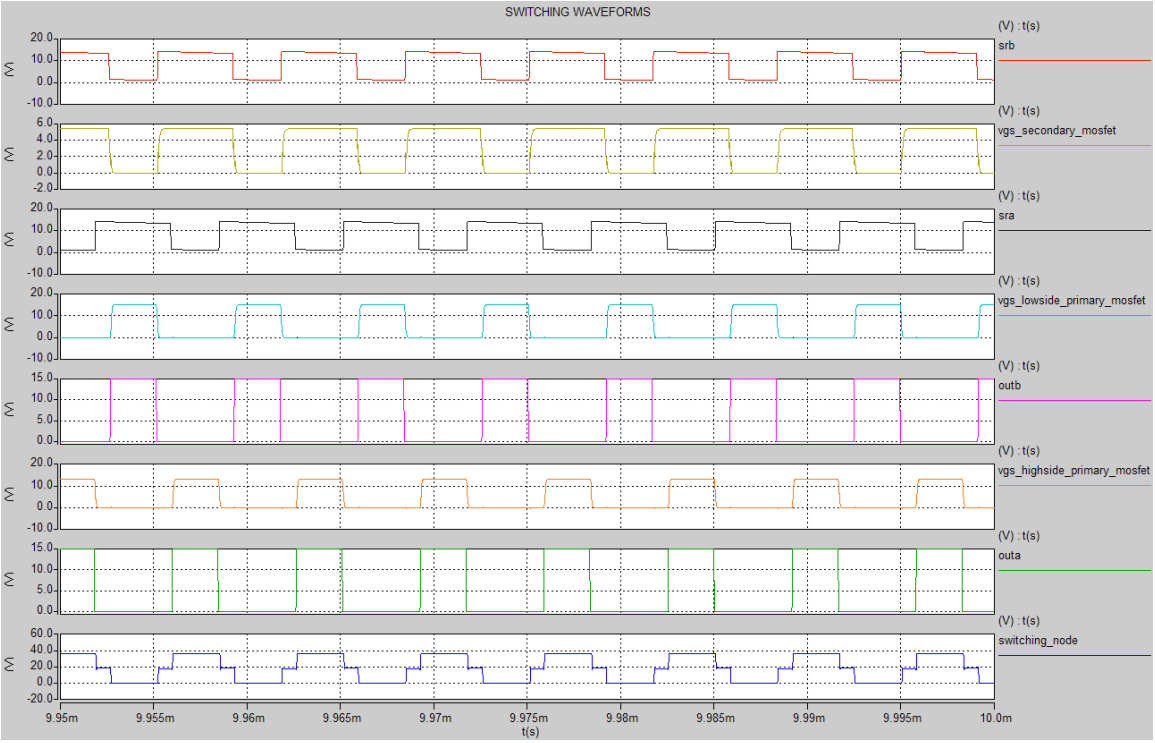


Figure 13: Graph result switching_waveforms (zoomed 9.95ms to 10ms) - ' transient analysis-36V input'

In Figure 13, we can view the switching_node voltage switches between (Vin/2) 18V and (Vin)36V based on the primary-side gate driver signals from controller `outa, outb` at a frequency of 150kHz and the duty controlled as required. The synchronous MOSFETs gate signals `sra` and `srb` are normally on and are only turned off when one of the primary MOSFETs is turned on.

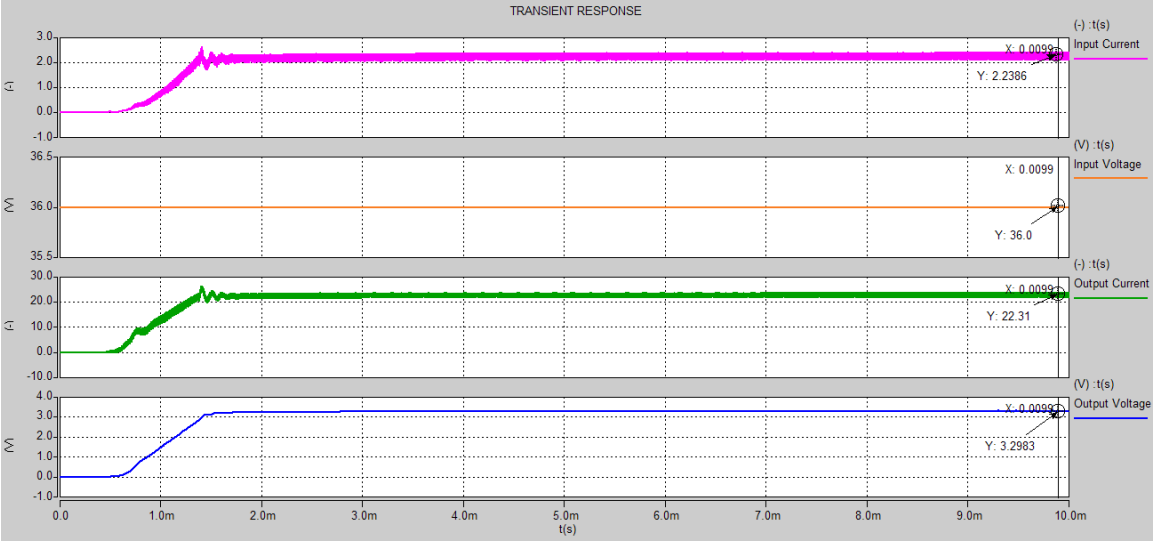


Figure 14: Graph result tr_analysis_output– 'transient analysis-36V input'

You can apply a `Vertical Marker` measurement at X =9.9m on the Graph result `tr_analysis_output`. In Figure 14, we can see that the Output Voltage is raising from 0V and has stabilized at 3.3V as required by the design specification with the load Current of 23A.

You can double-click on the Graph `additional_signals` to view `v_hicc`, `n_ilim`, `ss`, `sense_ct`- current at switching node signals during the transient analysis with 36V input.

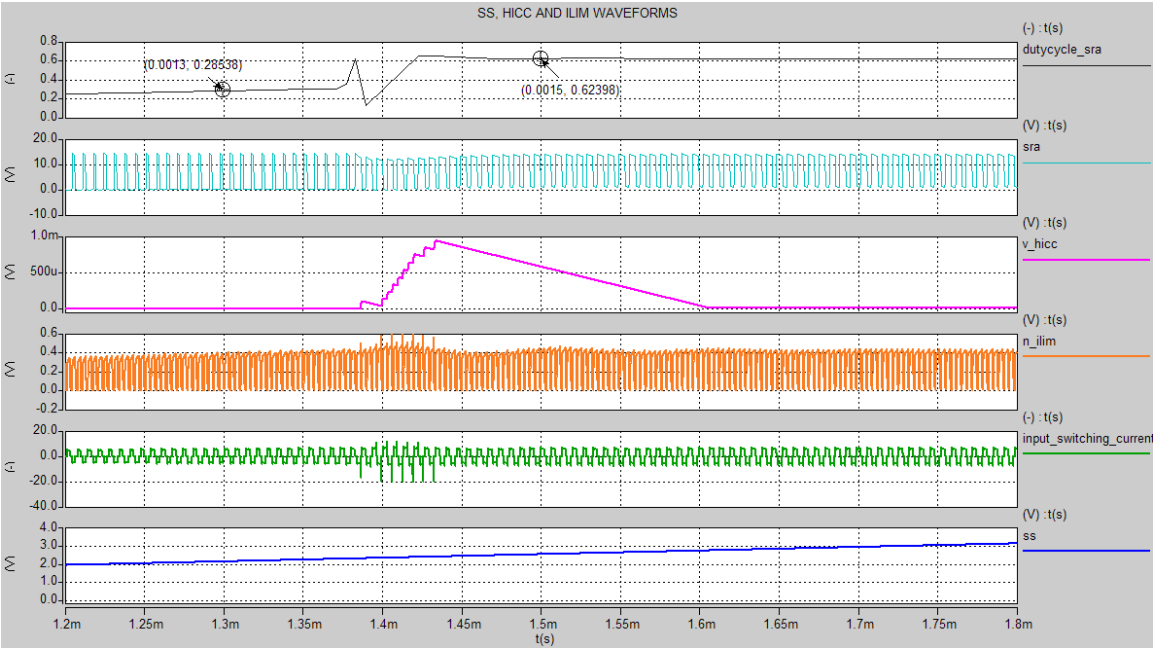


Figure 15: Graph result additional_signals (zoomed 1.2m to 1.8m)– 'transient analysis-36V input'

During the transition from soft-start mode to normal mode operation, the duty cycle of `sra` and `srb` increases. This change in the duty cycle causes an increase in the primary current. When this current goes beyond the cycle-by-cycle current limit, we observe an increase in voltage at HICC pin. In Figure 15, we see that voltage at `v_hicc` node momentarily increases as the input switching current crosses the cycle-by-cycle current limit. It resets once the current returns to steady-state within the designed cycle-by-cycle current limit operation time Toc.

5.1.3 TRANSIENT RESPONSE FOR INPUT VOLTAGES -36V,48V AND 72V AND OUTPUT LOAD CURRENT OF 23A

transient_analysis_vary_input_voltage.ai_exptlog

Task Label	Task Definition	De	Task Result	Task Statu
vary	vary -progress 500 -param :half_bridge_dc_dc_converter_v1:v_dc.vin:dc_value -type list -vlist {36 48 72} -q...		0 Failed	Complete
:half_bridge_dc_dc_converter_v1:v_dc.vin:dc_value=36				Complete
fosc	fosc = [frequency -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:ucc28250.ucc28250_1:clk -log yes]		301322.77668313	Complete
fsw_outa	fsw_outa = [frequency -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:outa -log yes]		150661.31930258	Complete
v_out_avg	v_out_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_out -xrange {x1 x2} -log yes]		3.300712212849	Complete
i_out_avg	i_out_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:i_out -xrange {x1 x2} -log yes]		23.085305392181	Complete
Pout	Pout = v_out_avg*i_out_avg		76.197949445321	Complete
v_in_avg	v_in_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_in -xrange {x1 x2} -log yes]		36.0	Complete
Pin	Pin = v_in_avg*i_in_avg		80.141095445058	Complete
Efficiency	Efficiency = (Pout/Pin)*100		95.079745319378	Complete
v_out_ripple	v_out_ripple = [peaktopeak -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_out -xrange {x1 x2} -log yes]		0.006434247979...	Complete
i_out_ripple	i_out_ripple = [peaktopeak -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:i_out -xrange {x1 x2} -log yes]		2.221402888701	Complete
:half_bridge_dc_dc_converter_v1:v_dc.vin:dc_value=48				Complete
fosc	fosc = [frequency -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:ucc28250.ucc28250_1:clk -log yes]		301322.77668329	Complete
fsw_outa	fsw_outa = [frequency -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:outa -log yes]		150670.15558262	Complete
v_out_avg	v_out_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_out -xrange {x1 x2} -log yes]		3.3006151565392	Complete
i_out_avg	i_out_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:i_out -xrange {x1 x2} -log yes]		23.082730020077	Complete
Pout	Pout = v_out_avg*i_out_avg		76.187208558569	Complete
v_in_avg	v_in_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_in -xrange {x1 x2} -log yes]		48.0	Complete
Pin	Pin = v_in_avg*i_in_avg		80.705045255146	Complete
Efficiency	Efficiency = (Pout/Pin)*100		94.402039324439	Complete
v_out_ripple	v_out_ripple = [peaktopeak -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_out -xrange {x1 x2} -log yes]		0.0122573510315	Complete
i_out_ripple	i_out_ripple = [peaktopeak -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:i_out -xrange {x1 x2} -log yes]		4.062392430375	Complete
:half_bridge_dc_dc_converter_v1:v_dc.vin:dc_value=72				Complete
fosc	fosc = [frequency -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:ucc28250.ucc28250_1:clk -log yes]		301322.77668329	Complete
fsw_outa	fsw_outa = [frequency -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:outa -log yes]		150641.44893277	Complete
v_out_avg	v_out_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_out -xrange {x1 x2} -log yes]		3.301045104584	Complete
i_out_avg	i_out_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:i_out -xrange {x1 x2} -log yes]		23.082124542288	Complete
Pout	Pout = v_out_avg*i_out_avg		76.195134223718	Complete
v_in_avg	v_in_avg = [average -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_in -xrange {x1 x2} -log yes]		72.0	Complete
Pin	Pin = v_in_avg*i_in_avg		83.83979654275	Complete
Efficiency	Efficiency = (Pout/Pin)*100		90.881821480645	Complete
v_out_ripple	v_out_ripple = [peaktopeak -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:v_out -xrange {x1 x2} -log yes]		0.0183818584746	Complete
i_out_ripple	i_out_ripple = [peaktopeak -pfile tr1 -signal :half_bridge_dc_dc_converter_v1:i_out -xrange {x1 x2} -log yes]		5.882471179658	Complete

Figure 16: Experiment report – 'transient analysis- input voltage sweep'

In Figure 16, we can see the measured results from the analysis run via `experiment transient analysis- input voltage sweep`, where the input voltage is set to 36,48 and 72V respectively.

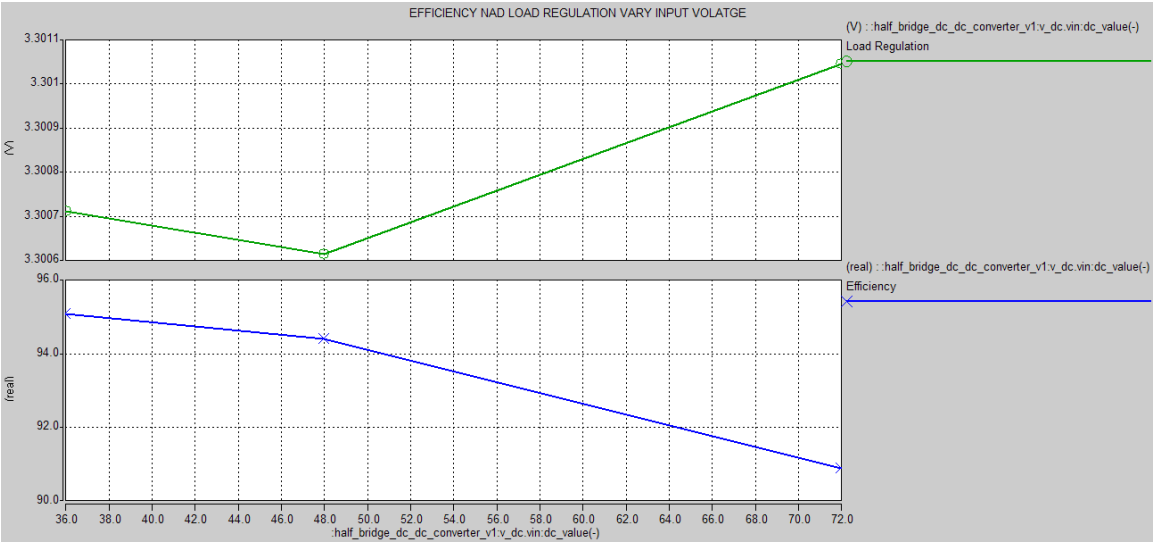


Figure 17: Graph result efficiency_regulation – 'transient analysis- input voltage sweep'

Figure 17 shows the Efficiency and Load Regulation variation, when input voltage is swept from 36 to 72V.

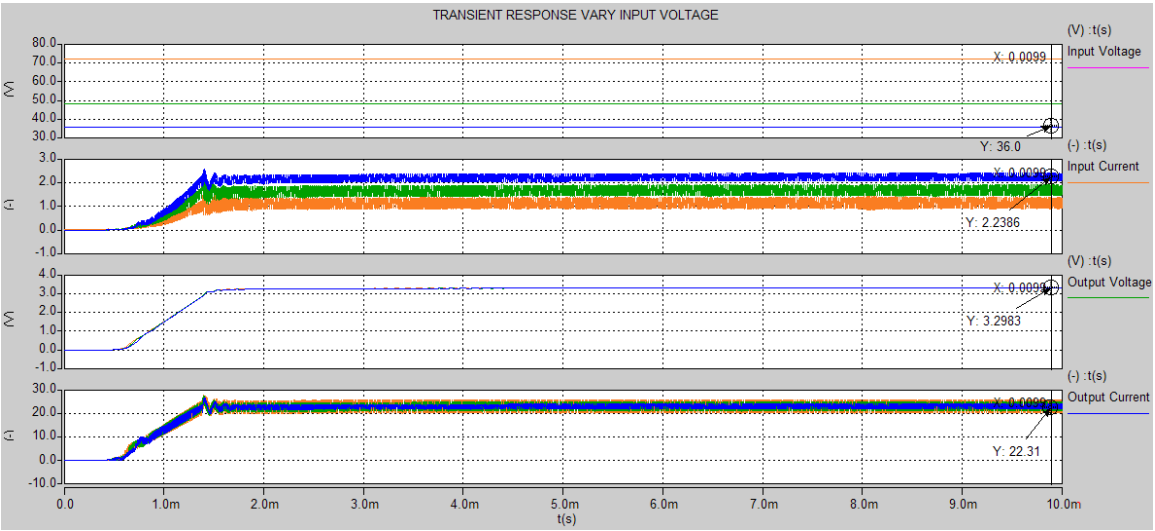


Figure 18: Graph result tr_analysis_output– 'transient analysis- input voltage sweep'

Figure 18 shows the input and output current and voltage waveforms with varied input voltage. A vertical marker can be applied at X=9.9m to measure the values on Graph.

5.1.4 SUMMARY OF SIMULATION RESULTS WITH NOMINAL CONDITIONS @ VIN=36V,48V,72V AND IOUT=23A

SPECIFICATIONS			Simulation results		
Name	Symbol	Nominal Value	Vin=36V	Vin=48V	Vin=72V
Output Voltage	Vout	3.3V	3.3007V	3.3006V	3.301V
Max Output Power	Pout max	75W	76W	76W	75W
Switching Frequency	Fsw	150kHz	150kHz	150kHz	150kHz
Max. Ripple Voltage on Vout	ΔVout	50mV	6.4mV	12.2mV	18.3mV
Pk-Pk Output Inductor Ripple Current	ΔIL	6.90A	2.221A	4.062A	5.88A
Output current	Iout	23A	23A	23A	23A
Efficiency at Full load	η	90%	95%	94%	90%

Table 3: Summary of Simulation results with nominal conditions @ Vin=36V,48V,72V

From the summary, we see that the overall design specification is met with varied input voltage and a load current of 23A.

5.1.5 EFFICIENCY AND LOAD REGULATION WITH VARY LOAD

Run the experiment `efficiency and load regulation` under the category `Efficiency_Load_Regulation` to validate the design for efficiency and load regulation at different loads.

In this experiment, we vary the load resistor `r_load` value from 0.143Ω to 0.825Ω to vary the load current correspondingly from 23A to 4A in 4 steps and the results are plotted.

Note: To boost the simulation speed for iterative analysis, we used the Multicore option in SaberRD. It enables the CPU to run parallel simulations of the loop by using multiple cores.

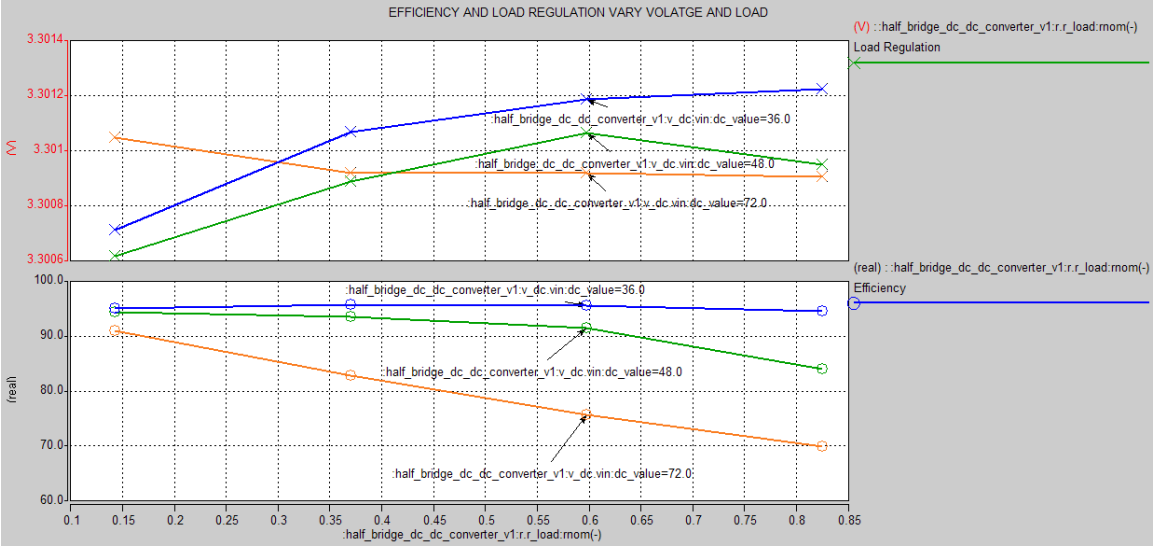


Figure 19: Graph result efficiency regulation – 'efficiency and load regulation'

Figure 19 shows the Efficiency and Load Regulation variation when load current is swept between no load to full load (in 4 steps) at input voltage of 36V,48V and & 72V respectively.

We can run the simulation with more load current vary steps to get more accurate efficiency variation from no load to full load. In summary, we see that the efficiency of the design is greater than 80% when the load current is more than 7A. The load regulation is less than 2% from no load to full load.

5.2 FAULT ANALYSIS FOR SHORT CIRCUIT LOAD AND OVER VOLTAGE CONDITIONS

A fault set `short_load_ovp` is created by using the Fault Tool and added to the experiment `load short and ovp`. The simulation is run with an input voltage of 72V. This experiment tests the design when load is shorted and when input over voltage conditions occur.

Faults

Fault Set: short_load_ovp

Configure Faults

Include	ID	Fault	Type	Parameter	Non-Fault Value	Fault Value	Fault Begin	Fault End	Description
☑	OV_momentary	/v_dc.Vin dc_value	Parametric	dc_value	36	**75**	**10m**	**11m**	Over voltage from 10m to 11m
☐	short_load_infinite	/r.r_load p,m short	Analog Pin	rnom	100meg	**1u**	**8m**	inf	Fault short load from 8ms to inf
☐	short_load_momentary	/r.r_load p,m short	Analog Pin	rnom	100meg	**1u**	**5m**	**5.5m**	Fault short load from 2ms to 2.5ms

Concurrent Fault Groups

Include	Group	Fault List	Description
☑	short_load	short_load_infinite,short_load_momentary	Fault short load momentary from 5ms to 5.5ms and from 8m to infinite

Figure 20: Fault set short_load_ovp used in Experiment- 'load short and ovp'

The Fault- `OV_momentary` (highlighted in red box), introduces a fault input over voltage of 75V at 5ms and ends at 6ms to analyze the over voltage protection function of the controller. The concurrent Fault `short_load` (highlighted in yellow box at the bottom), is created to introduce `short_load_momentary` and `short_load_infinite` in a single simulation loop. In this concurrent fault loop, the load is shorted between 5ms to 6ms and then again from 8ms to end of the simulation to analyze the controller and design behavior under these fault conditions.

5.2.1 EXPERIMENT SETUP FOR SHORT LOAD FAULT ANALYSIS

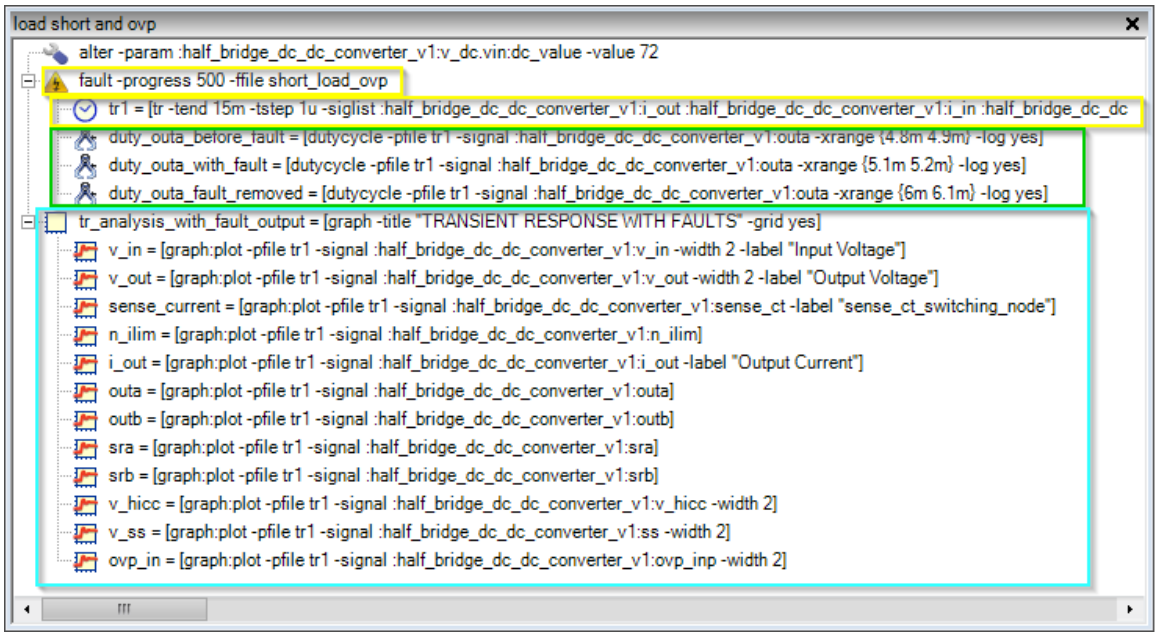


Figure 21: Experiment for faults- 'load short and ovp'

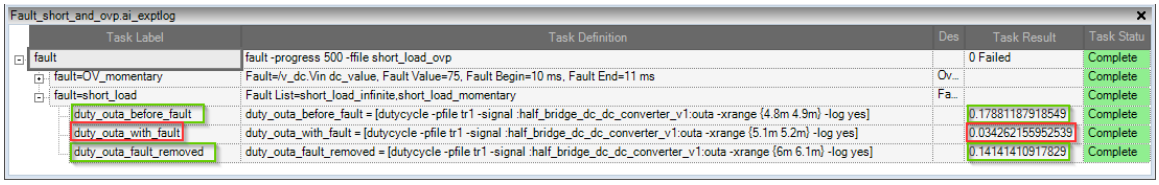


Figure 22: Experiment report - 'load short and ovp'

From Figure 22, we can see that the duty cycle of the switching MOSFETs (`outa`) is reduced compared to the normal operating duty cycle once the short load/Over current fault is detected. Once the overcurrent fault is removed at 5.5ms, the duty cycle returns to normal for the switching MOSFETs since the controller has not entered into Hiccup mode.

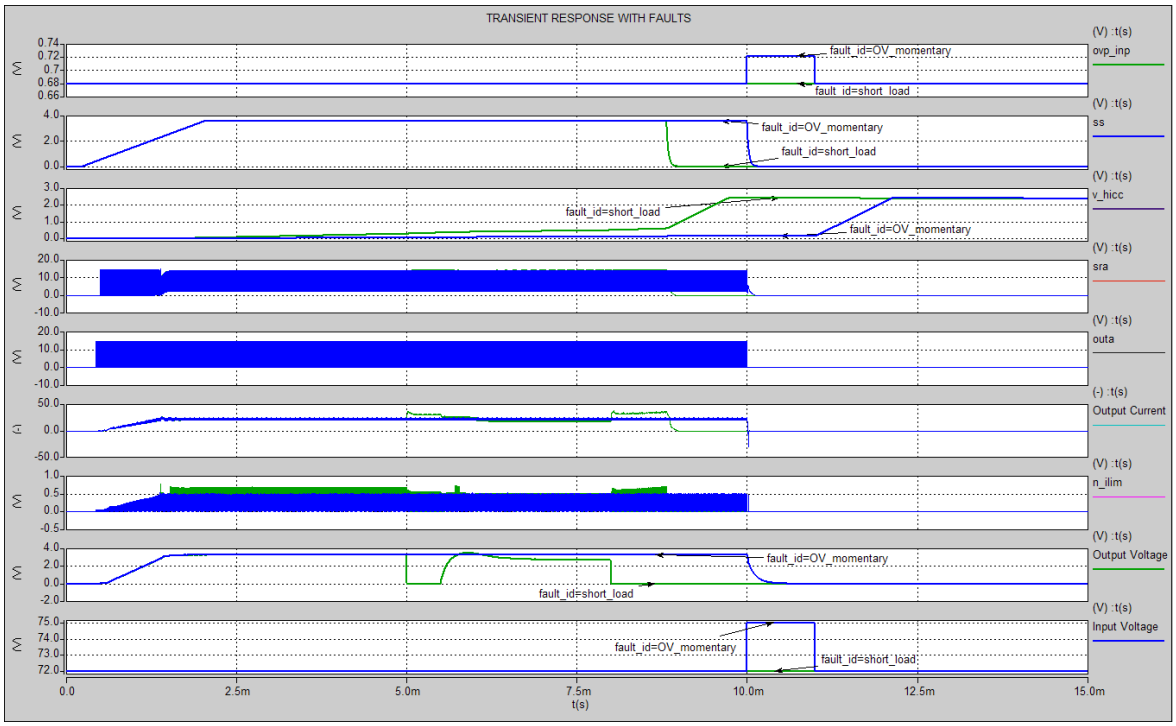


Figure 23: Graph result – 'load short and ovp'

In Figure 23, the signals in blue corresponds to the Fault- `OV_momentary` and the signals in Green corresponds to the Fault-`short_load`.

Shorted Load fault summary

From the results, we can see that the voltage at pin HICC (`v_hicc`) starts increasing and the duty cycle of switching MOSFETs is reduced once the current limit is triggered at 5ms as the load is shorted. If the cycle-by-cycle current limit condition continues, HICC pin reaches 0.6 V, and all four outputs `outa`, `outb`, `sra` and `srb` are shut down. Since the first fault introduced here is for only 0.5ms, the `v_hicc` has not reached 0.6V. Hence, the Hiccup mode for the controller is not yet triggered and the circuit operates back in normal mode, once the fault is ended at 5.5ms.

When the short load fault is introduced again for a longer time from 8ms, we can see that `v_hicc` reaches 0.6V, and hence the UCC28250 enters Hiccup mode. UCC28250 shuts down and no longer gives the switching pulses `outa`, `outb`, `sra`, and `srb`. The `v_hicc` quickly increases to 2.4V and `SS` pin is pulled to ground internally.

From this point, the Chicc starts discharging till the voltage at HICC pin, `v_hicc` reaches 0.3V. If the fault persists beyond this point, a new Hiccup cycle would start.

Thus, the over current protection functionality of the controller UCC28250 in the design is validated as per the datasheet, which is shown in the below Figure 24.

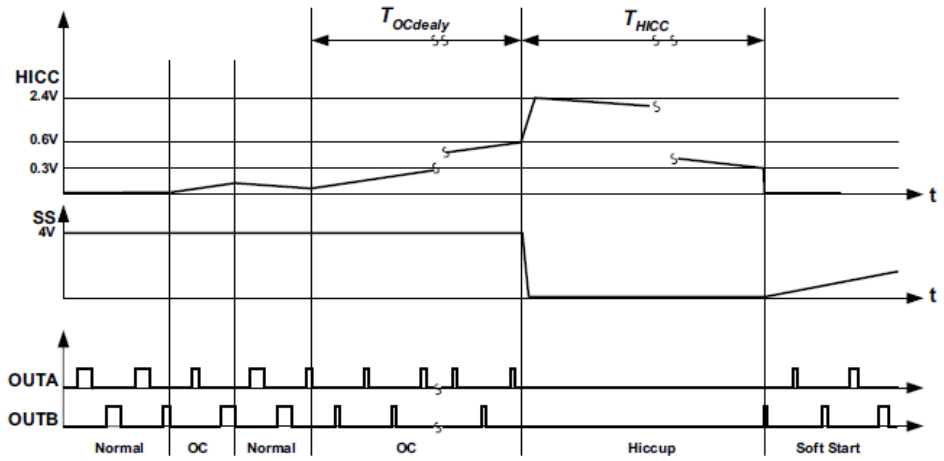


Figure 24: Cycle-by-Cycle Current Limit Delay Timer and Hiccup Restart Timer[1]

Over Voltage fault summary

From Figure 23, we can see that the voltage at OVP pin, `ovp_in` exceeds 0.7V when the over voltage fault is applied at 5ms. The controller is turned OFF and the outputs `outa, outb, sra, and srb` stop switching. `SS` pin is pulled to ground internally. Once the fault is removed at 6ms, the controller enters hiccup mode.

A soft-start cycle begins after hiccup cycle is finished. Thus, the over voltage protection functionality of the controller UCC28250 has been validated with this fault simulation.

6 Conclusion

In this example, a symmetrical half-bridge DC-DC converter with primary-side voltage mode control is designed by using the UCC28250 with the required specifications. The secondary side is a control driven synchronous rectifier. The design is tested for varied input voltages against the design specifications. The efficiency and load regulation over the input voltage variation has been tested. The Hiccup mode protection and Over voltage protection of controller UCC28250 model has been verified in the design using Fault analysis from SaberRD.

The half-bridge topology is a good choice due to the optimized voltage rating for the primary-side MOSFETs, full utilization of the transformer core and the extremely high effective duty cycle[4].

The design can be further enhanced to include temperature variation of the components, especially switching devices to analyze the efficiency and load regulation of the converter for varied temperatures. Loop Response for the feedback compensation circuit- Gain and Phase can be analyzed.

Going further, you can design, optimize and validate other converter configurations by using the UCC28250 Saber model. Examples:

- Half-Bridge DC-DC converter with secondary side control with an output pre-bias condition with voltage mode control.
- Half-Bridge DC-DC converter with secondary side control with an output pre-bias condition current mode control.
- Also, other topologies can be realized like Full-bridge, Interleaved forward and Push-pull.

7 References

[1]. http://www.ti.com/lit/ds/symlink/ucc28250.pdf
[2]. http://www.ti.com/lit/ug/sluu429b/sluu429b.pdf
[3]. https://www.powerelectronics.com/power-management/smart-rectification-benefits-half-bridge-converters
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