Synchronous Buck Converter Using UCC3882

SaberRD design Example

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Contents

Introduction

Synchronous Buck converter topology has advantage of improved efficiency over nonsynchronous buck converter due to lower voltage drop at low-side MOSFET when compared to power diode of nonsynchronous buck converter. Synchronous buck converter has made its presence in high efficiency applications like battery charger for Laptops, Voltage Regulator Modules (VRM) in motherboards of PCs and laptops, power audio amplifier, quadcopter, brushed and brushless motor controllers.

This design example illustrates the operation of synchronous buck converter in Pentium 2 processor where the DC-DC converter is controlled by current mode synchronous controller UCC3882. The design example showcases legacy design given in application note of UCC3882 (available in working directory) where Power MOSFETs uses TO-220 packaging. With the help of SaberRD advanced simulation techniques, it is found that lead inductance present due to power MOSFET packing is causing more switching loss and thereby efficiency is reduced. Using Power MOSFET tool, it can be proven through simulation that by providing better packaging for MOSFETs, efficiency can be improved in synchronous buck converter.

A snapshot of the schematic is given in Figure 1.

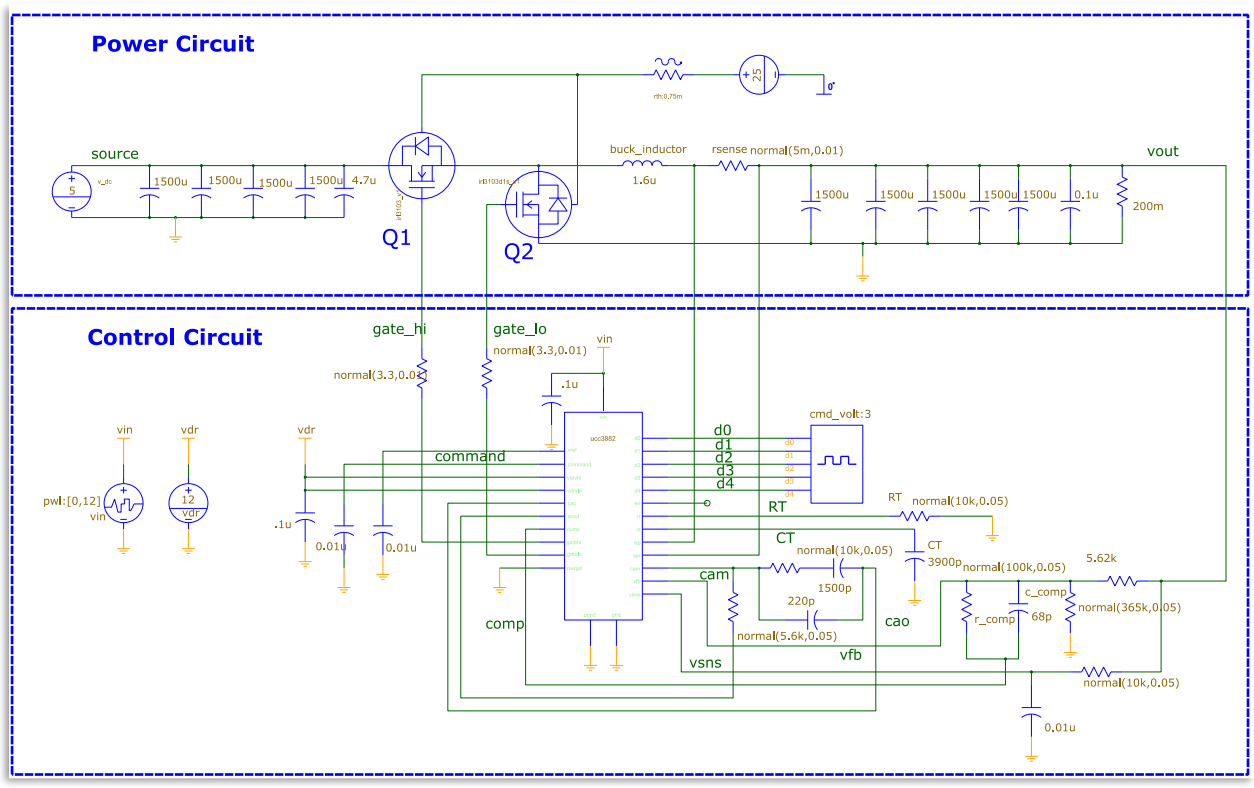


Figure 1: Schematic of Synchronous Buck Converter Using UCC3882

The synchronous buck converter consists of High Side MOSFET (Q1) and Low Side MOSFET (Q2), gate driver IC, input capacitors and output LC filter. The PWM signal is typically generated from a control IC. The example utilizes the `ucc3882.sin` from Components library in SaberRD, for the control IC. The MOSFET models `irl3103_v1.sin` and `irl3103d1s_v1.sin` used in the design are characterized

from manufacturer datasheet using Power MOSFET Tool in SaberRD. The MOSFETs turn on and off signal is driven using the control IC UCC3882 through closed feedback loop to control the output voltage.

The design example is available with test benches created using Experiment Analyzer in SaberRD that helps to automate analysis, post processing measurements and pass/fail test conditions to check whether design specifications are met or not. Initially, when design specifications are tested, it is found that High side MOSFET is dissipating more power and converter efficiency is less than 90%. The design example explains the investigation carried out and steps to improve efficiency. Later, more analysis like Six Sigma quality check on output voltage and operation during Under Voltage Lock Out (UVLO) are carried out using Experiment Analyzer.

Advanced feature like Distributive Iterative Analysis (DIA) is utilized in this design example to improve the throughput of the test benches having iterative analysis. The iterative analysis definition in experiment analyzer allows the users to specify the number of parallel runs that need to be performed during DIA. SaberRD will distribute each runs of the iterative analysis to different cores depending on parallel runs and completes the simulation in a shorter time. One of the test benches takes 26 mins to complete in a dual-core machine whereas, it takes only 10 mins in quad-core machine using DIA. It is approximately 1.5X speedup in quad-core machine. The distribution of parallel runs can be monitored through the Job Monitor window in SaberRD. A comparative study on the performance using DIA is also discussed in this design example.

Principle of Operation of Synchronous Buck Converter

Figure 2 explains the simplified switching behavior of a synchronous buck converter. The ratio (output voltage)/(input voltage) is controlled by the duty cycle of Q1. The buck inductor and output capacitors in Figure 2 forms a low pass filter. This low pass filter smooths out the MOSFET switching action and produces a smooth DC output voltage. When Q1 is turned on (Ton), Q2 is turned off and output current flows through buck inductor. And when Q1 is turned off (Toff), Q2 is turned on, the current through the buck inductor is free wheeled through Q2 as shown in Figure 2. Figure 3 explains the ideal circuit waveforms with no dead time.

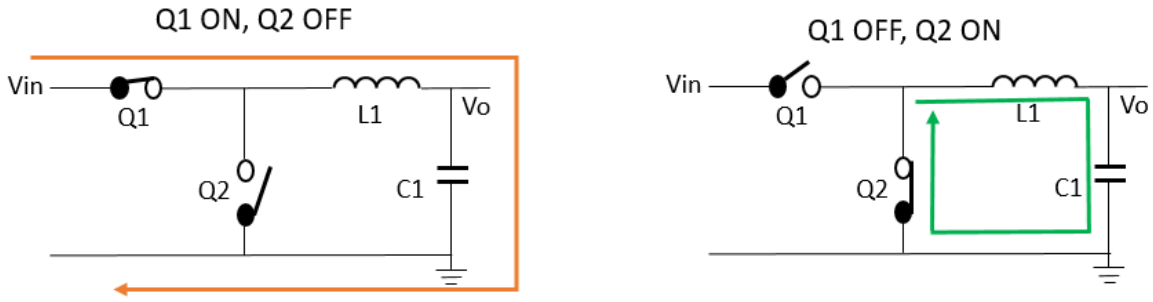


Figure 2: Simplified Switching Behavior

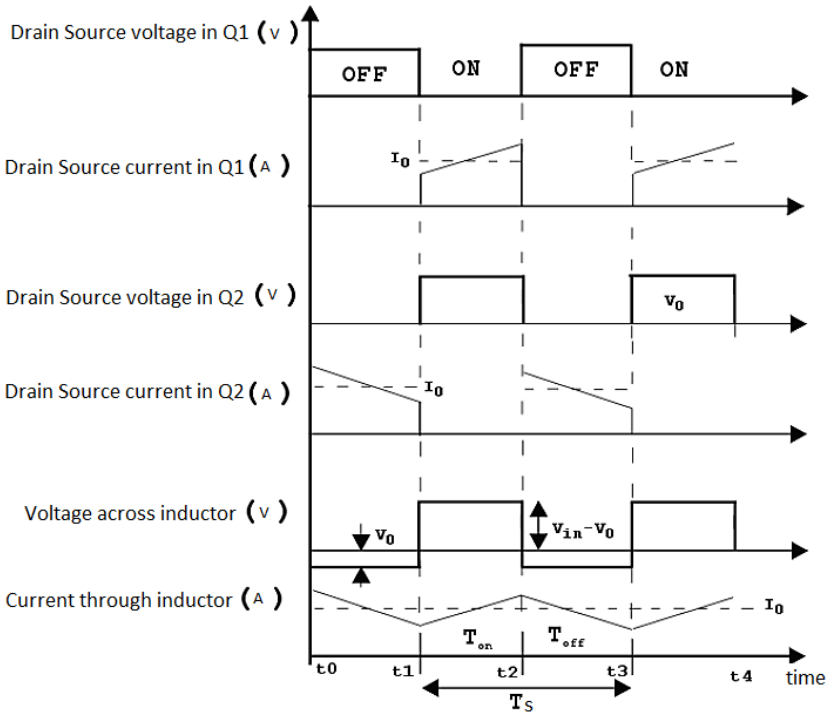


Figure 3: Ideal circuit waveforms with no dead time [3]

In order to maintain safe and efficient operation of Synchronous buck converter, both MOSFETs, Q1 and Q2 should never be turned on at same time. There should be good amount of dead time between when Q1 is turned off and Q2 is turned on and vice versa to avoid cross conduction. It is also desirable to reduce the dead time to a minimum to improve efficiency. However, dead time should not go below the turn-on and turn-off times of Q1 and Q2. Figure 4 explains the simplified Switching State diagram. The switching sequence should be A-B-C-B-A for safe and efficient operation of the converter.

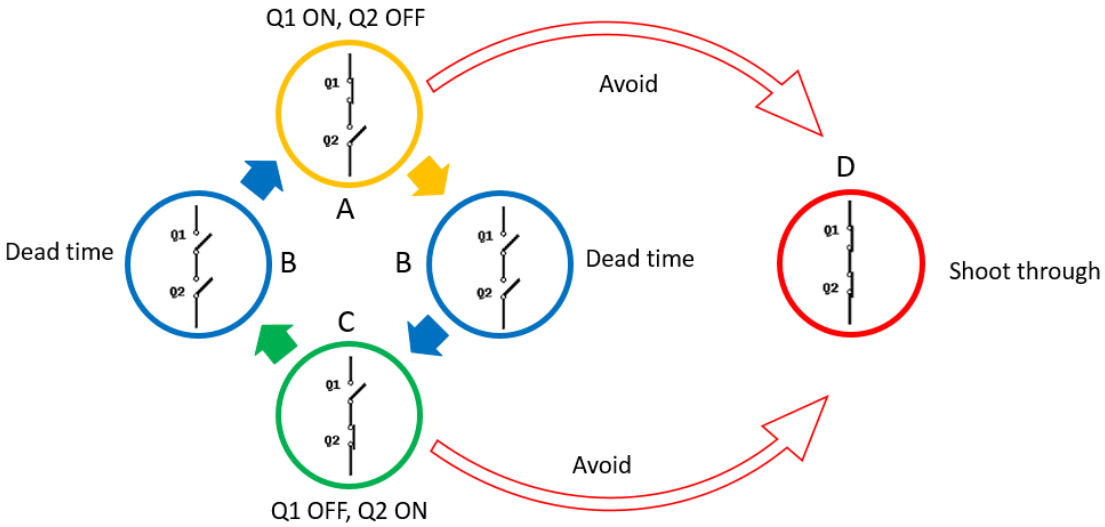


Figure 4: Simplified Switching State Diagram

Usage of UCC3882

Block diagram of UCC3882 is given in Figure 5.

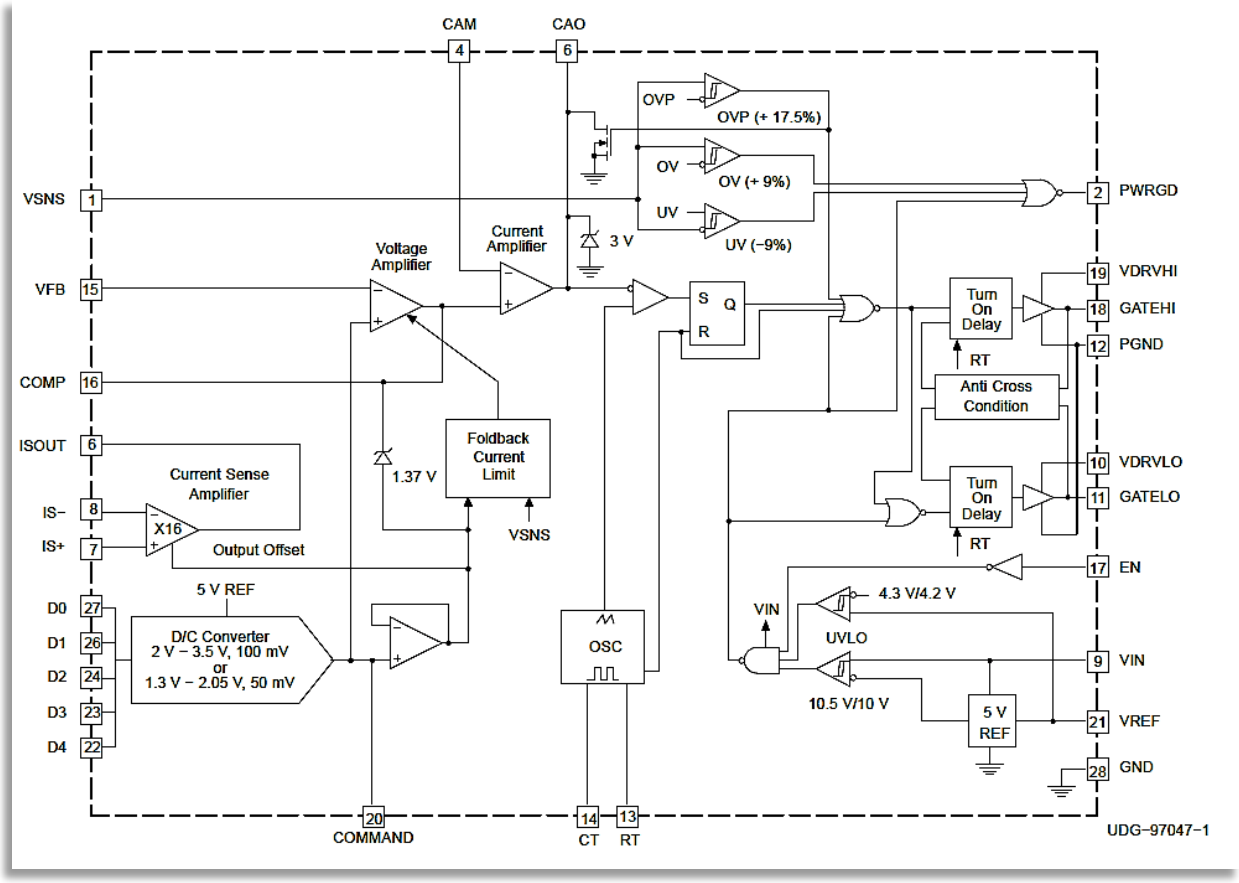


Figure 5: Block diagram of UCC3882 [1]

The reference command is provided to 5-bit DAC which is programmed based on the table look up given in the application note of UCC3882 (available in working directory as ucc3882-1.pdf). A snapshot of the table is given in Figure 6 for ready reference. As per the application note, the DAC covers 1.3V to 2.05V in 50mv steps and 2.1V to 3.5V in 100mV steps. In this design, a custom MAST model `cmd_reference.sin` is used to provide 5-bit digital output depending on the reference voltage required. The model is designed to take input from 2.3V to 3.0V in 100mV steps and give 5-bit digital output based on the look up table.

Table 1. Programming the Command Voltage for the UCC3882

Digital Command					Command Voltage	GATEHI/GATELO Status	Digital Command					Command Voltage	GATEHI/GATELO Status
D4	D3	D2	D1	D0			D4	D3	D2	D1	D0		
0	1	1	1	1	1.300	Note 1 ?	1	1	1	1	1	2.000	Note 1 ?
0	1	1	1	0	1.350	Note 1 ?	1	1	1	1	0	2.100	Enabled
0	1	1	0	1	1.400	Note 1 ?	1	1	1	0	1	2.200	Enabled
0	1	1	0	0	1.450	Note 1 ?	1	1	1	0	0	2.300	Enabled
0	1	0	1	1	1.500	Note 1 ?	1	1	0	1	1	2.400	Enabled
0	1	0	1	0	1.550	Note 1 ?	1	1	0	1	0	2.500	Enabled
0	1	0	0	1	1.600	Note 1 ?	1	1	0	0	1	2.600	Enabled
0	1	0	0	0	1.650	Note 1 ?	1	1	0	0	0	2.700	Enabled
0	0	1	1	1	1.700	Note 1 ?	1	0	1	1	1	2.800	Enabled
0	0	1	1	0	1.750	Note 1 ?	1	0	1	1	0	2.900	Enabled
0	0	1	0	1	1.800	Enabled	1	0	1	0	1	3.000	Enabled
0	0	1	0	0	1.850	Enabled	1	0	1	0	0	3.100	Enabled
0	0	0	1	1	1.900	Enabled	1	0	0	1	1	3.200	Enabled
0	0	0	1	0	1.950	Enabled	1	0	0	1	0	3.300	Enabled
0	0	0	0	1	2.000	Enabled	1	0	0	0	1	3.400	Enabled
0	0	0	0	0	2.050	Enabled	1	0	0	0	0	3.500	Enabled

Figure 6: Table look up for programming the command voltage [1]

The output of the DAC is compared with system output voltage through VFB pin using a voltage error amplifier. The error difference is fed to current amplifier where the current from Rsense (from schematic) is compared and the output is sent to the PWM generator. The PWM generator creates gate signals for both MOSFETs. The oscillating frequency is set as 225kHz using external resistor (R_T) and external capacitor (C_T). The Anti-Cross Condition block eliminates cross conduction internally by programming the dead time between turn-off and turn on of the external high side MOSFETs.

There are overvoltage and under-voltage comparators monitoring the system output voltage and indicates when it rises above or falls below its designed value by more than 9% [1]. A second overvoltage comparator digitally forces GATEHI off and GATELO on when the system output voltage exceeds its designed value by more than 17.5% [1]. UCC3882 is provided with Under Voltage Lock Out (UVLO) protection for the input voltage (VIN pin). The threshold values of UVLO are given as below.

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis		300	500	700	mV

Figure 7: UVLO ratings as per datasheet of UCC3882 [1]

When the voltage at VIN pin of UCC3882 goes below 10.5V, UVLO is activated and GATEHI and GATELO pins are disabled. During that period UCC3882 will not drive the MOSFETs and the output voltage starts to drop. When the voltage at VIN pin increases and exceeds 10V, UVLO is released and UCC3882 starts to drive the MOSFET. This behavior is explained in detail in the Simulation and Analysis section.

MOSFET Characterization

MOSFET models used in this example are characterized using Power MOSFET tool in SaberRD release M-2017.06. Characterized curves for high side MOSFET model (`irl3103_v1.sin`) are shown in Figure 8.

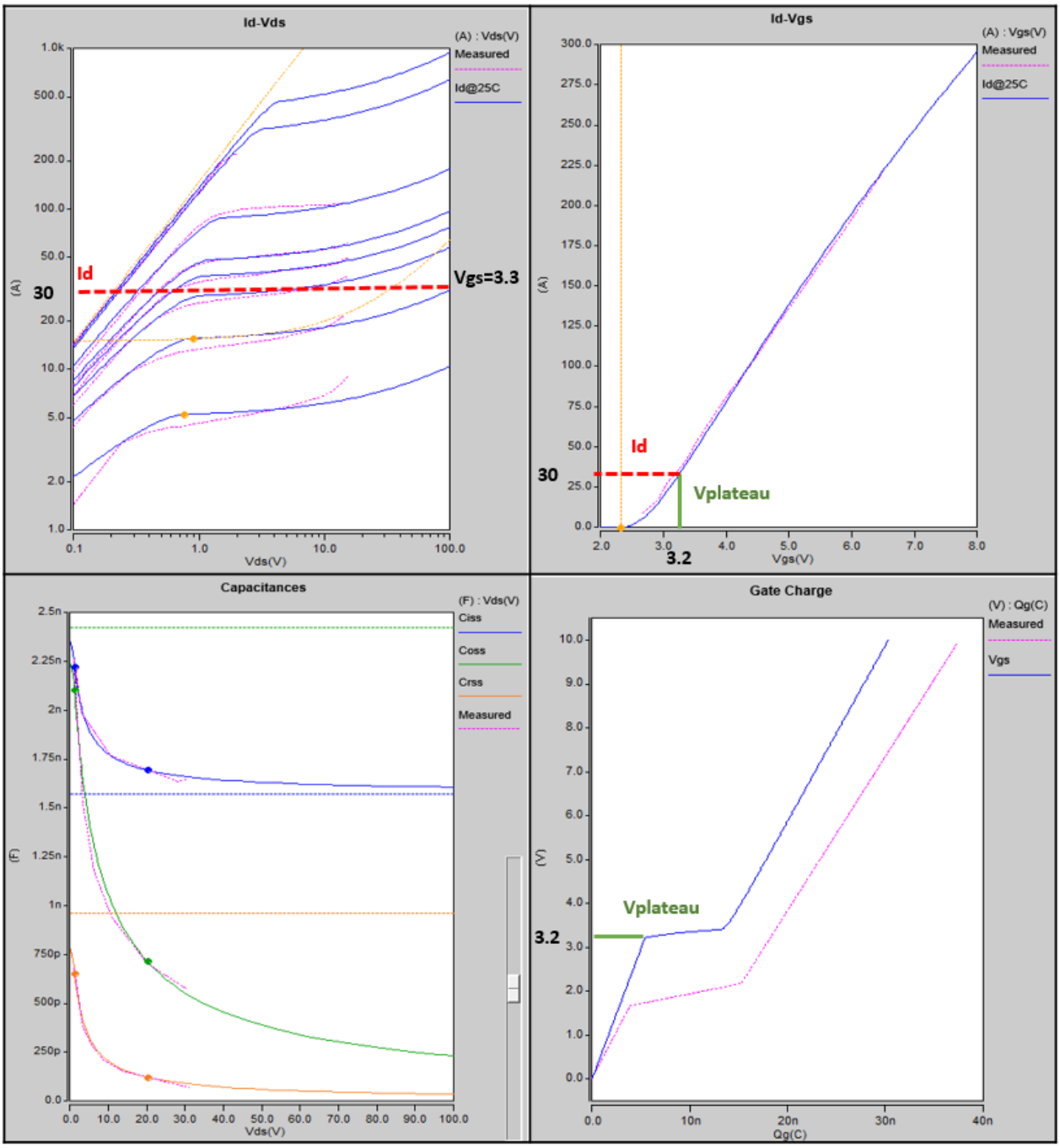


Figure 8: Characterization curves of irl3103_v1.sin

NOTE: It can be seen in Figure 8 that gate charge curve is not matching with the datasheet curves though other curves are closely matching. But the measurement values of Vplateau and Id as shown

in Figure 8 gives indication that the optimized curve for gate charge obtained in tool is in accordance with other curves. This shows that there is some inconsistency with datasheet curve for gate charge. But tool was able to optimize the gate charge parameters based on other parameters from capacitor, Id-Vgs and Id-Vds curves.

Characterized curves for low side MOSFET (`irl3103d1s_v1.sin`) are shown in Figure 9.

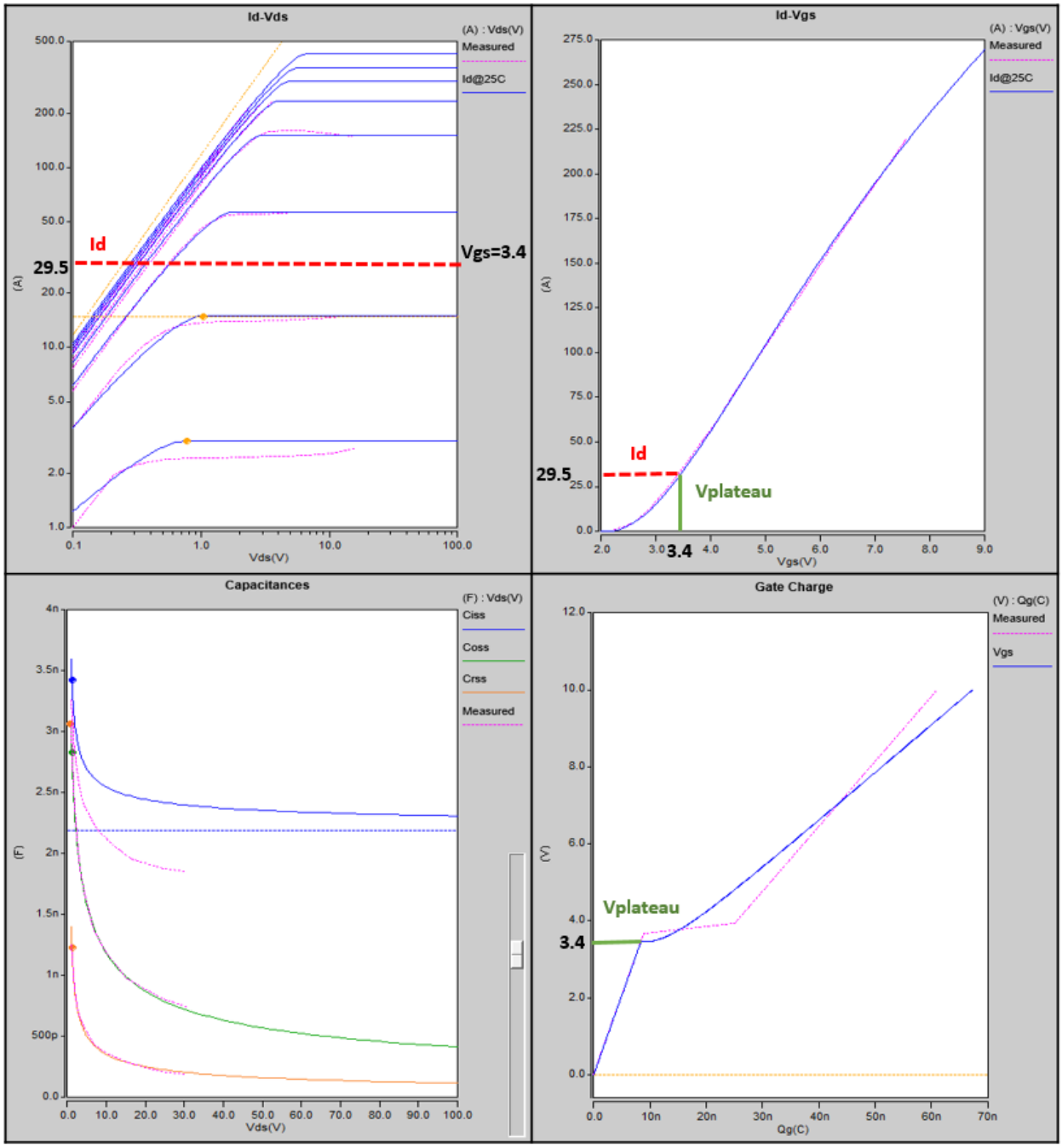


Figure 9: Characterization curves of irl3103d1s_v1.sin

NOTE: In this model, better match is achieved by optimizer for gate charge curve but some tradeoff is made in capacitor curves.

Tool also provides facilities to add stress measures, tolerance rating and thermal network in the models created. The stress ratings properties in Power MOSFET tool are highlighted in red as shown in Figure 10. And the region highlighted in orange and green shows the tolerances rating and thermal network respectively.

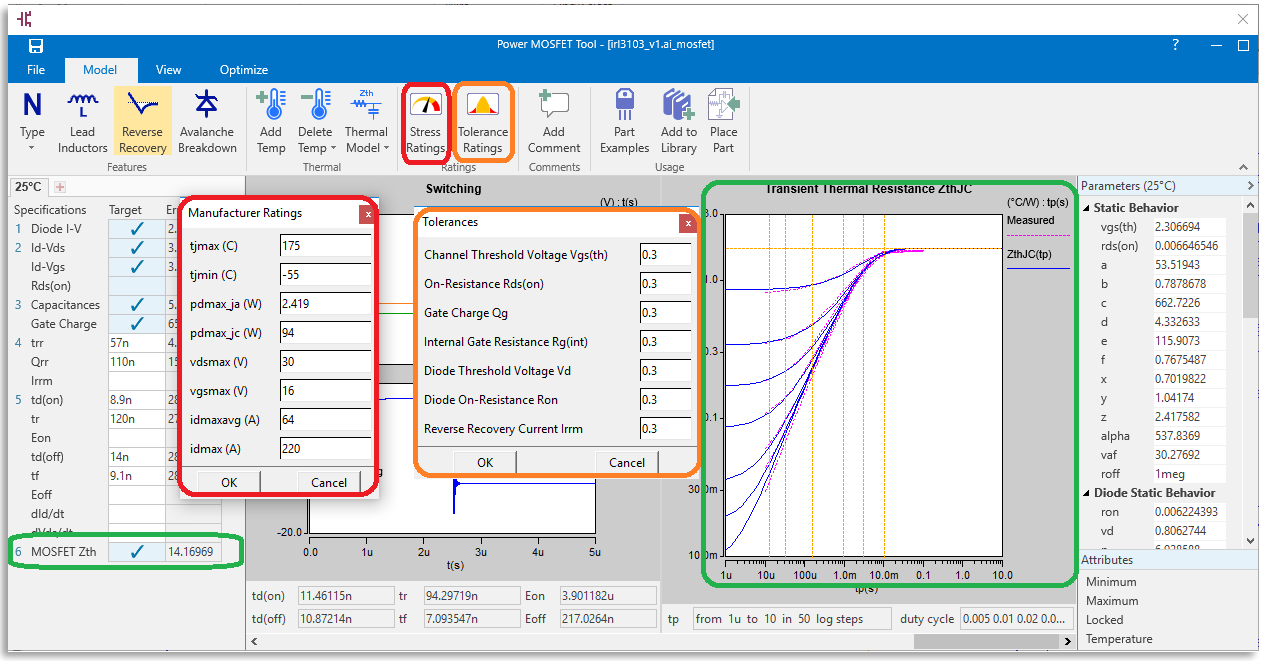


Figure 10: Power MOSFET tool with stress rating, tolerances and thermal network

Detailed information regarding characterization of MOSFET are available in tool documentation. Power MOSFET tool > File > Help> Tool Documentation.

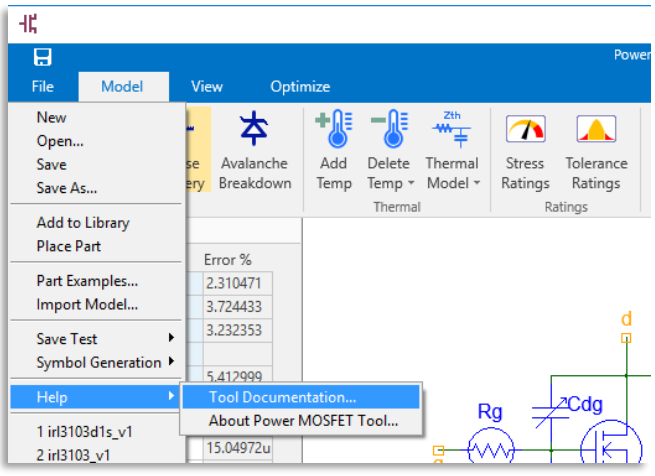


Figure 11: Help link from Power MOSFET tool

Simulation and Analysis

The simulation and post processing is carried out through automated test benches created using Experiment Analyzer in SaberRD. There are five test benches for this design example as given below.

1) Check design specification using nominal analysis (*exp1_nominal_analysis.ai_expt*)
2) Compare system efficiency with respect to load current (*exp2_efficiency_vs_load_current.ai_expt*)
3) UVLO operation of UCC3882 (*exp3_UVLO.ai_expt*)
4) Check Six Sigma quality on output voltage by varying design parameter considering extreme values using Monte-Carlo analysis (*exp4_six_sigma.ai_expt*)

How to run experiments

1) *Open the design **sync_buck_conv.ai_dsn** from attached design folder.*
2) *On the Simulate tab, select Experiment from the Analysis list.*
3) *Select the Experiment of interest from the list as shown below.*

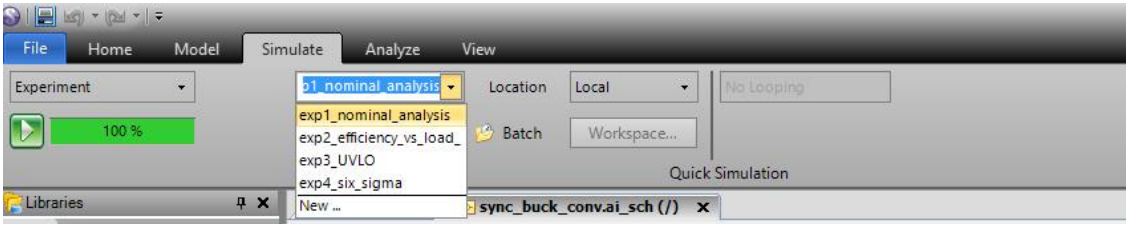


Figure 12: Simulate tab where experiments can be selected for simulation

4) *Click the GO button*  .

Advantage of Using Distributed Iterative Analysis (DIA)

Experiments *exp2_efficiency_vs_load_current.ai_expt* and *exp4_six_sigma.ai_expt* contains iterative analyses that takes long time to complete the simulation. SaberRD can utilize the multiple cores available in multi-core computers to distribute each individual runs of an iterative analysis to different cores and completes the simulation in much shorter time. DIA settings available in iterative analysis is shown in Figure 13. In Figure 14, comparative results on time taken and speed up are shown for two experiments when they are executed in dual-core and quad-core machines using DIA feature.

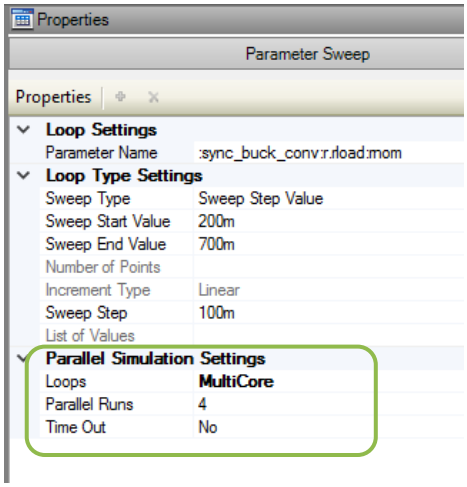


Figure 13: Properties tab of iterative analysis where parallel simulation settings can be defined.

Experiment Name	*exp2_efficiency_vs_load_current.ai_exp*		*exp4_six_sigma.ai_exp*	
	Time taken (min)	Performance boost w.r.t to sequential run (speed up)	Time taken (min)	Performance boost w.r.t to sequential run (speed up)
Dual core machine (Sequential)	26	-	160	-
Dual Core machine (Multicore, parallel runs - 4)	15	1.7 X	96	1.6 X
Quad core machine (Multicore, parallel runs - 4)	10	2.6 X	45	3.5 X

Figure 14: Comparison of simulation time and speed up with respect to number of cores and parallel runs

It can be seen that when multi-core is used, the time taken to simulate the iterative analysis has reduced. Therefore, more number of cores with relevant number of parallel runs can speed up the simulation and increase the throughput in a significant way.

1) Nominal analysis

In Nominal Analysis test bench (*exp1_nominal_analysis.ai_expt*), time domain (transient) analysis is performed under normal operating conditions. The amount of electrical and thermal stress on power switching devices are also analyzed in this experiment using Stress analysis. VIN pin of UCC3882 is provided with 12V and system input voltage (node name - source) is set to 5V. Design specifications to be met are given below.

a) Output voltage = 3V ± 5%
b) Output current = 15A ± 5%
c) Switching frequency = 225kHz ± 5%
d) Maximum overshoot = 9% of set voltage value = 3 * 0.09 = 0.27V
e) Efficiency >90%
f) Power switches shouldn't be stressed (electrical and thermal) above the rated value.

Details of experiment with brief description of each section is given in Figure 15 and Figure 16 respectively.

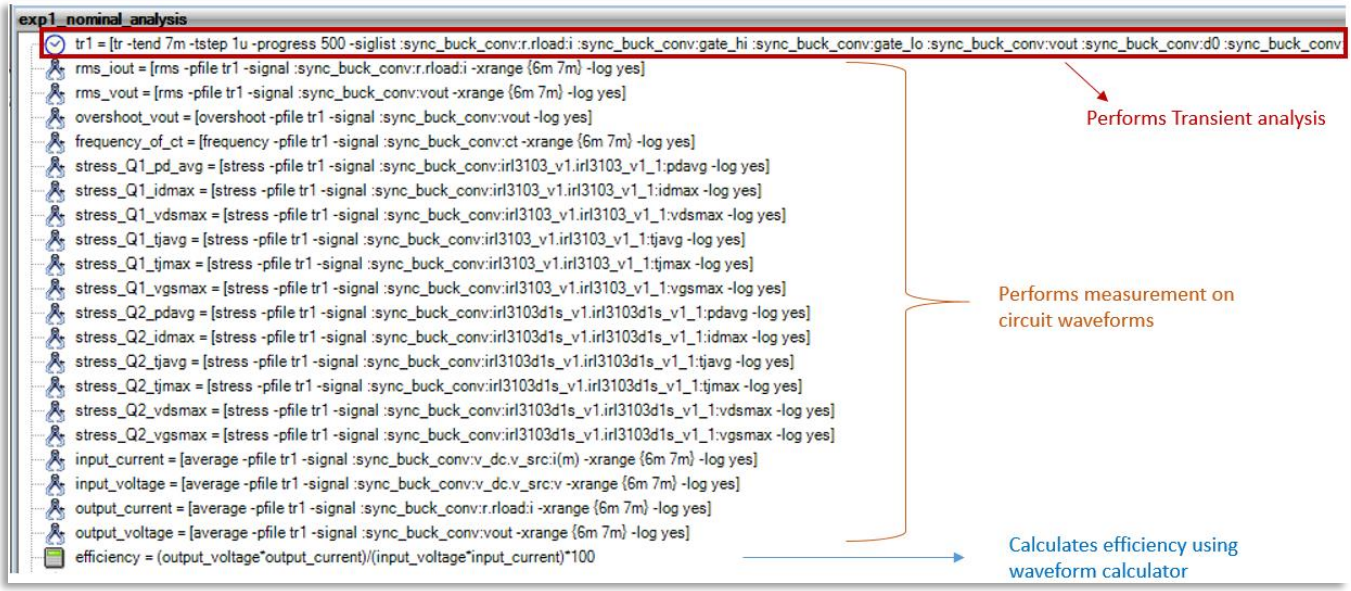


Figure 15: Simulation and measurements in Experiment exp1_nominal_analysis.ai_expt

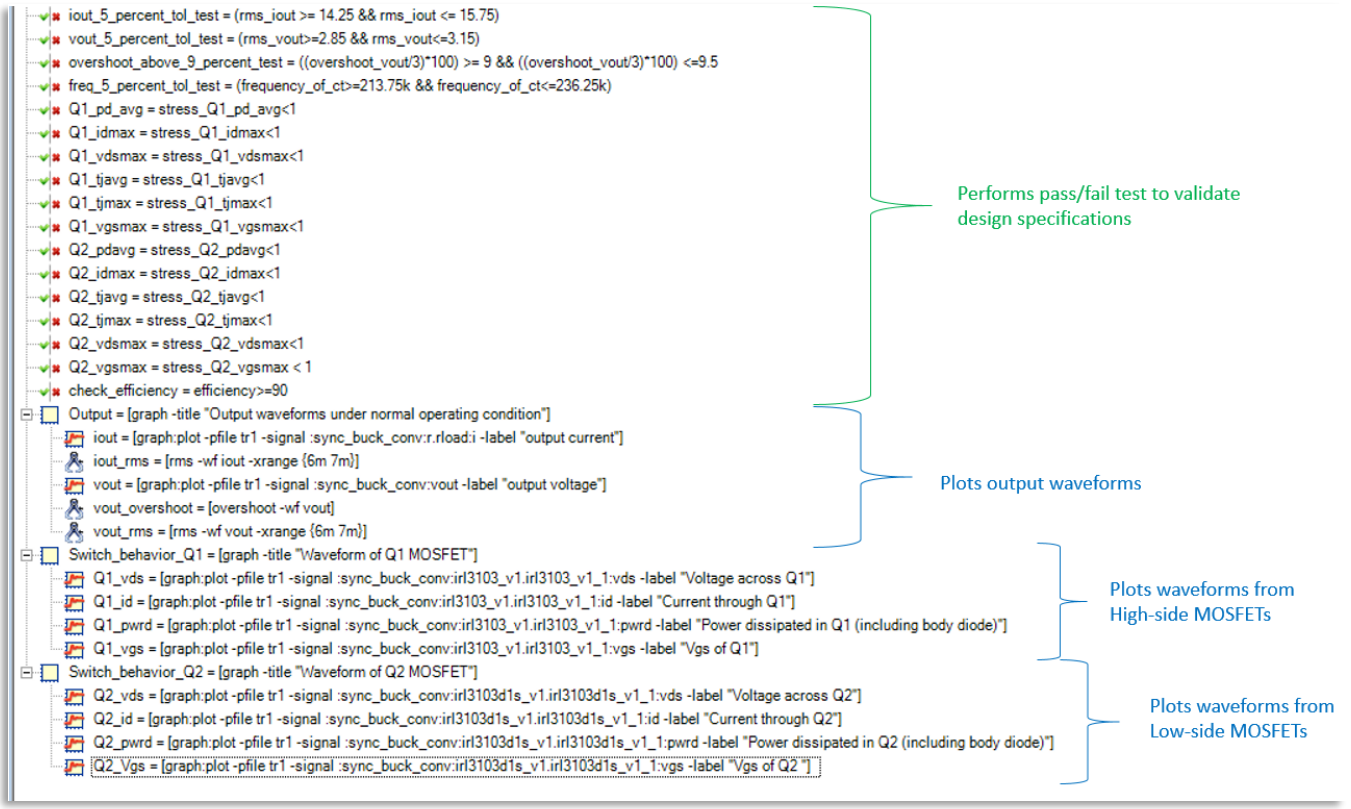
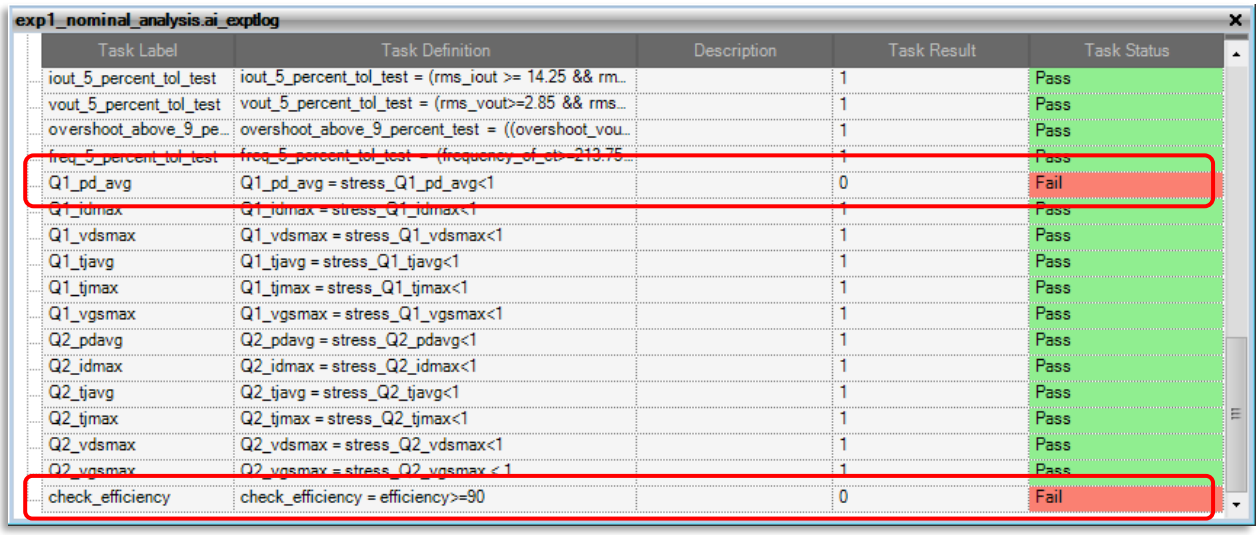


Figure 16: Pass/Fail tests and graphs in Experiment exp1_nominal_analysis.ai_expt

After successful completion of simulation, the results are loaded in Results Tab. When experiment report is opened from Results Tab, it can be seen that Efficiency is <90% and power dissipated in High-side MOSFET is more than the rated value as shown in Figure 17.



exp1_nominal_analysis.ai_exptlog

Task Label	Task Definition	Description	Task Result	Task Status
iout_5_percent_tol_test	iout_5_percent_tol_test = (rms_iout >= 14.25 && rm...		1	Pass
vout_5_percent_tol_test	vout_5_percent_tol_test = (rms_vout>=2.85 && rms...		1	Pass
overshoot_above_9_pe...	overshoot_above_9_percent_test = ((overshoot_vou...		1	Pass
freq_5_percent_tol_test	freq_5_percent_tol_test = ((frequency_of_ct>=213.75...		1	Pass
Q1_pd_avg	Q1_pd_avg = stress_Q1_pd_avg<1		0	Fail
Q1_idmax	Q1_idmax = stress_Q1_idmax<1		1	Pass
Q1_vdsmax	Q1_vdsmax = stress_Q1_vdsmax<1		1	Pass
Q1_tjavg	Q1_tjavg = stress_Q1_tjavg<1		1	Pass
Q1_tjmax	Q1_tjmax = stress_Q1_tjmax<1		1	Pass
Q1_vgsmax	Q1_vgsmax = stress_Q1_vgsmax<1		1	Pass
Q2_pdavg	Q2_pdavg = stress_Q2_pdavg<1		1	Pass
Q2_idmax	Q2_idmax = stress_Q2_idmax<1		1	Pass
Q2_tjavg	Q2_tjavg = stress_Q2_tjavg<1		1	Pass
Q2_tjmax	Q2_tjmax = stress_Q2_tjmax<1		1	Pass
Q2_vdsmax	Q2_vdsmax = stress_Q2_vdsmax<1		1	Pass
Q2_vgsmax	Q2_vgsmax = stress_Q2_vgsmax<1		1	Pass
check_efficiency	check_efficiency = efficiency>=90		0	Fail

Figure 17: Experiment report from exp1_nominal_analysis.ai_expt

Detailed Stress report including derated value, actual stressed value and time of occurrence is generated from Stress analysis and report can be opened from Results Tab as shown in Figure 18.

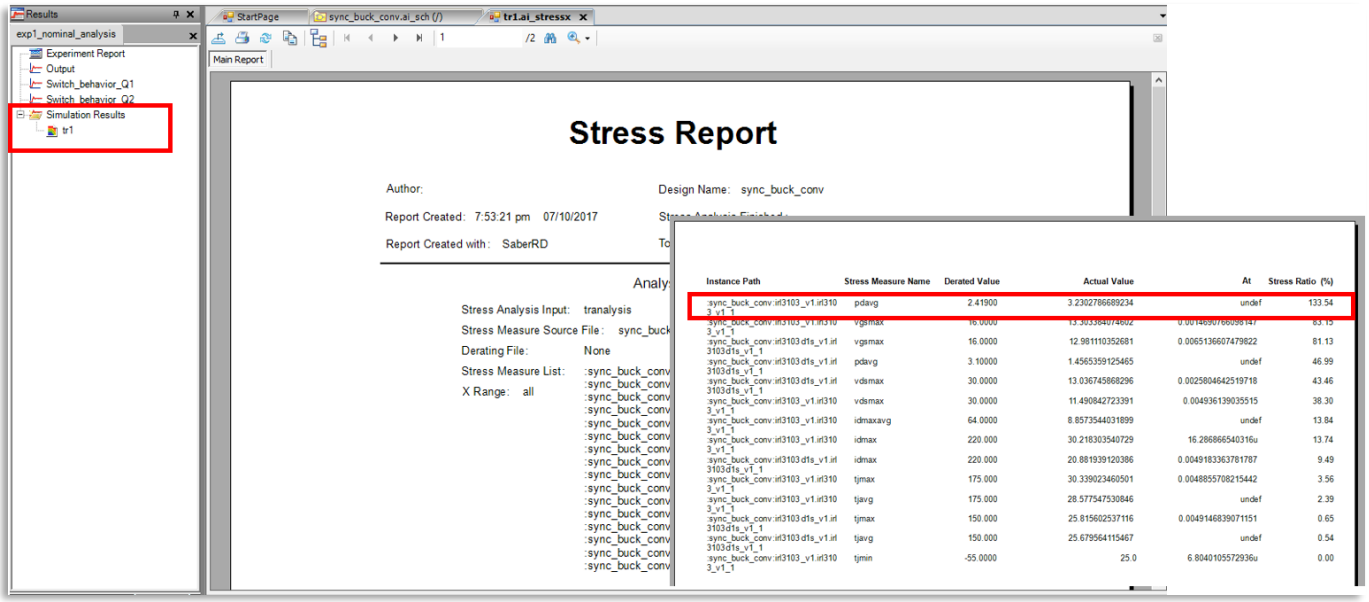


Figure 18: Stress report from exp1_nominal_analysis.ai_expt

Let's investigate the reason behind it high power dissipation at High Side MOSFET. Open the graph "Switch_behavior_Q1" from the Results Tab. To have a close look on the waveform, zoom

into a region in steady state by changing axis properties from Properties tab as shown in Figure 19. It is seen that the power dissipated is more during turnoff period.

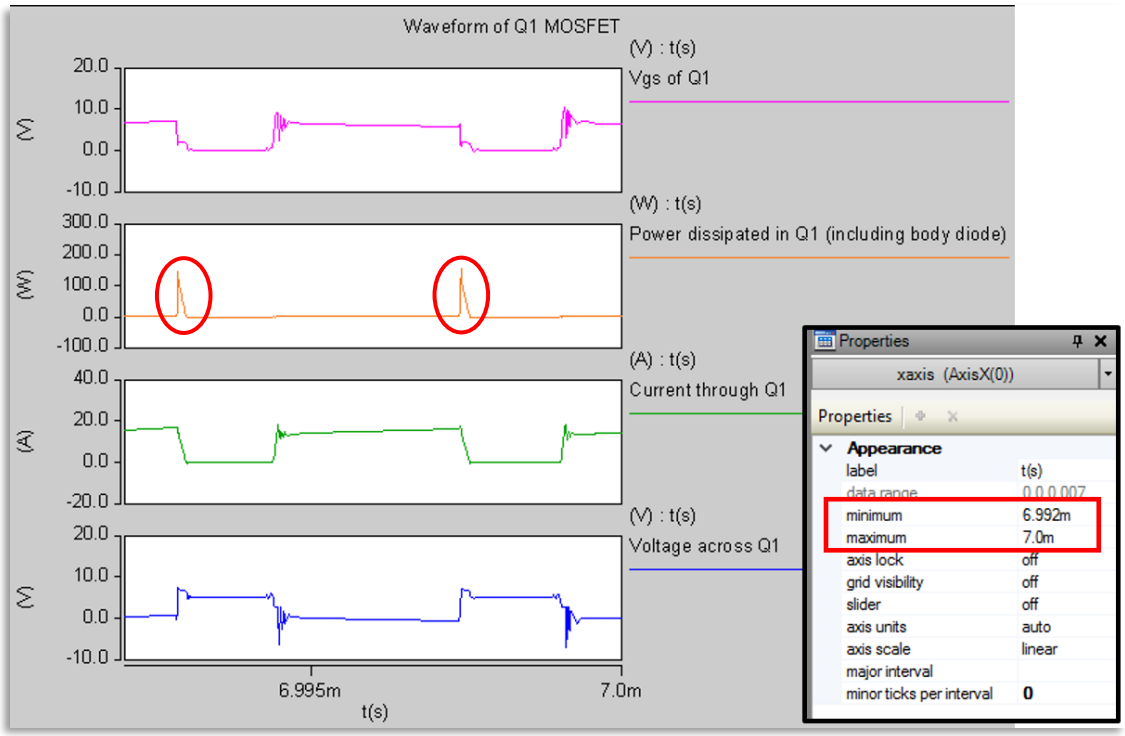


Figure 19: Zoomed in graph Switch_behavior_Q1

Let's zoom into turnoff period and place voltage and current waveforms superimposed as shown Figure 20.

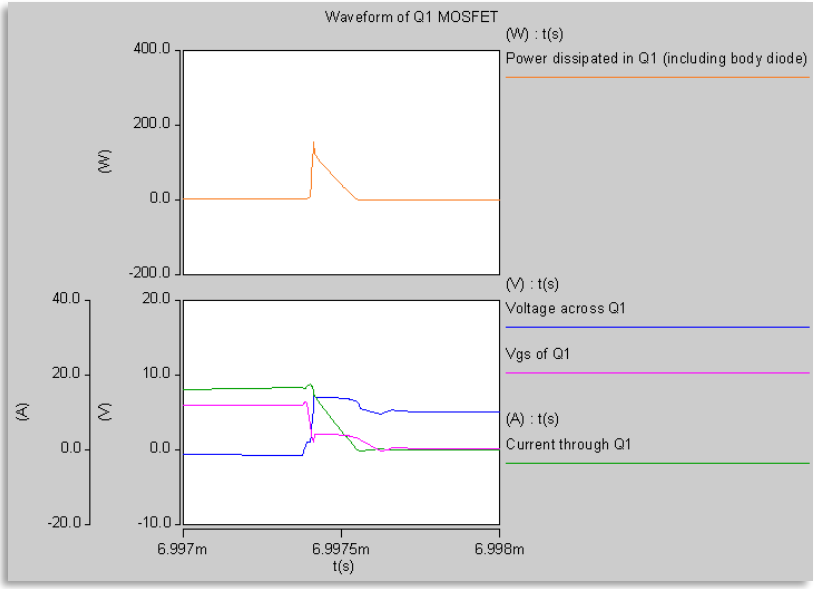


Figure 20: Zoomed in close to Turn off time

Now, it is very clear that during turnoff, the voltage across the Q1 MOSFET reaches 100% of its value when gate is turned off but current through the device takes time to become zero. When Q1 is turned off, the decreasing current in Q1 forces a negative voltage across source inductance of Q1 MOSFET. And at same time when Q2 is turned on, the current flows through Q2 via drain inductance of Q2. The presence of high source and drain inductance of Q1 and Q2 respectively, creates delay in transfer of energy during turn off. The TO220 packaging of MOSFET has high lead inductance whose range varies from 1n to 10n.

Solution

The effect of common source inductance can be avoided by improving the packaging of MOSFETs for synchronous buck converter [2]. TI has Power MOSFET blocks with advanced packing known as SON (Small Outline No Lead) where the High and Low side MOSFETs are connected without having a source and drain inductance as shown below.

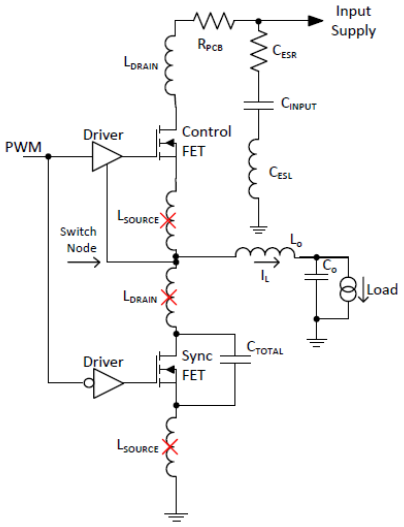


Figure 21: TI power blocks [2]

This can be modeled using Power MOSFET tool in SaberRD by removing the lead inductance of both MOSFETs. Open both MOSFETs in Power MOSFET tool from Properties tab as shown in Figure 22. And click Lead Inductors toggle button as shown in Figure 23.

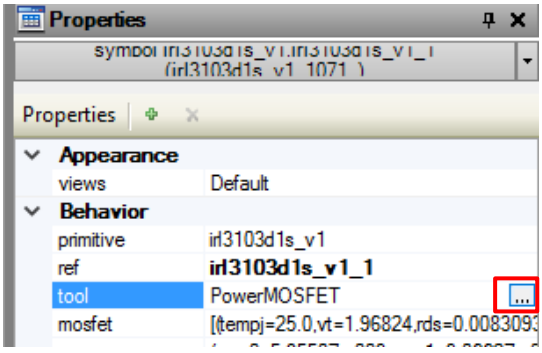


Figure 22: Properties of a MOSFET model created by Power MOSFET tool

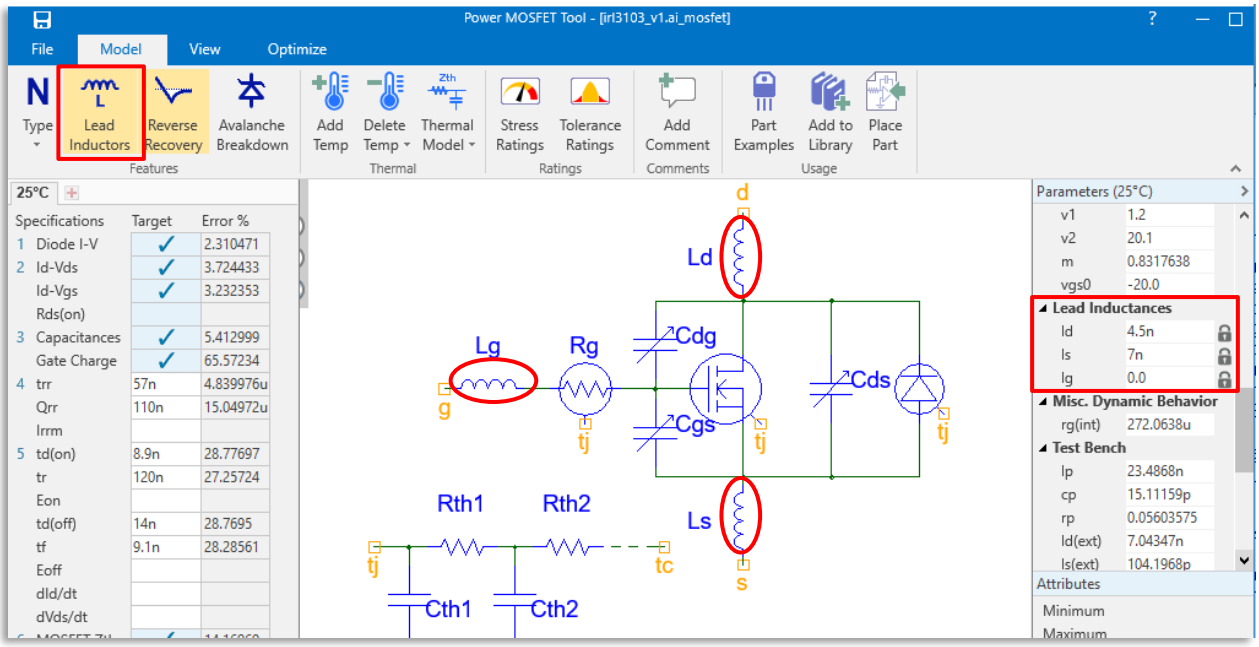


Figure 23: Power MOSFET tool with Lead inductors.

Now, the lead inductors are removed from the MOSFET model. Save both MOSFET models and run the *exp1_nominal_analysis.ai_expt* again. Open the experiment report and Switch_behavior_Q1 graph from Results Tab and it can be seen that all design specifications are met and efficiency is also above 90%.

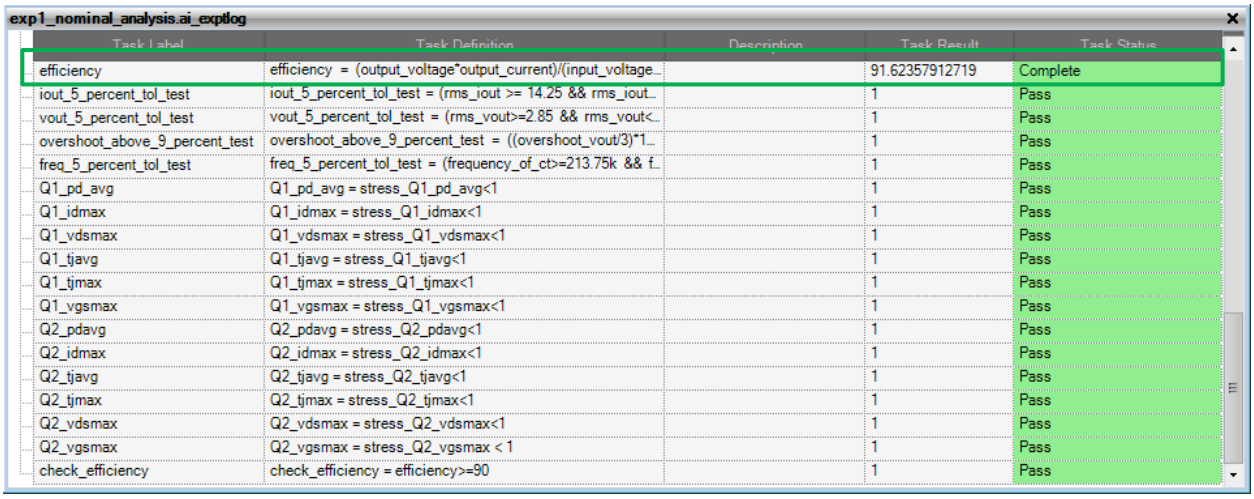


Figure 24: Experiment report after Lead inductors are removed

Now, if zoomed into turnoff period as shown in Figure 25, it can be seen that the turn off period is less and drain current becomes zero when voltage across the MOSFET reaches 100%. Therefore, the switching power loss is reduced and thereby increasing the efficiency.

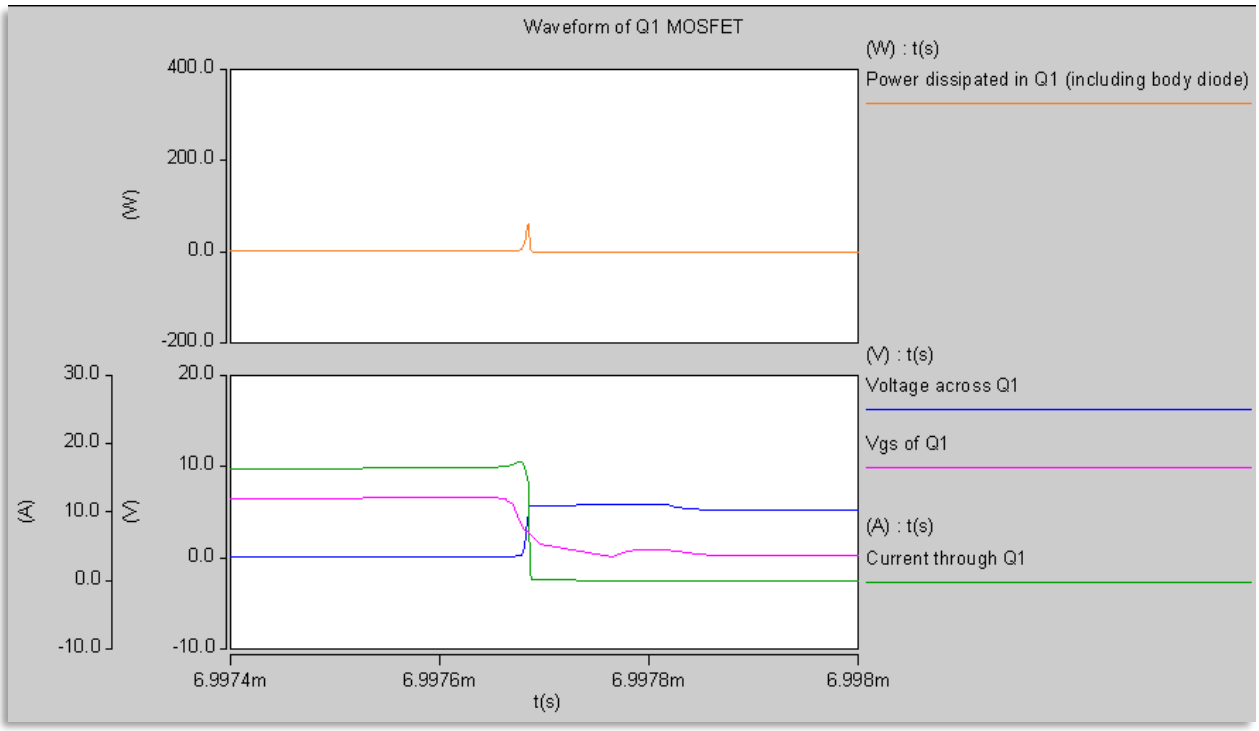


Figure 25: Waveform from graph "Switch_behavior_Q1" after Lead Inductors is removed

2) Compare system efficiency with respect to load current

In experiment *exp2_efficiency_vs_load_current.ai_expt*, the efficiency of the system is calculated and plotted across various load currents. Details of experiment with brief description of each section is given in Figure 26.

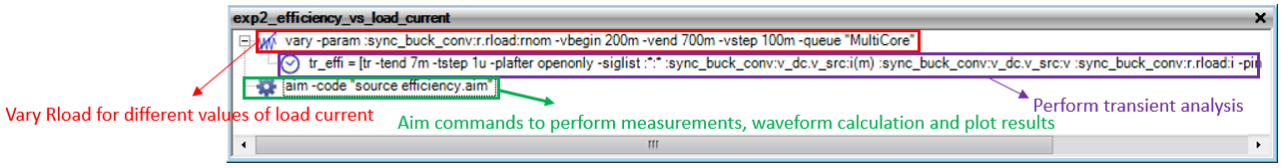


Figure 26: Experiment setup for exp2_efficiency_vs_load_current.ai_expt

It will take some time to complete the simulation depending on the number of parallel runs explained earlier.

After successful completion of simulation, the graphs are loaded automatically through AIM codes as shown in Figure 27. It can be seen that the efficiency has increased when lead inductors are excluded in MOSFET models. This shows that if packing is improved with less lead inductance, the efficiency can be improved in synchronous buck converter.

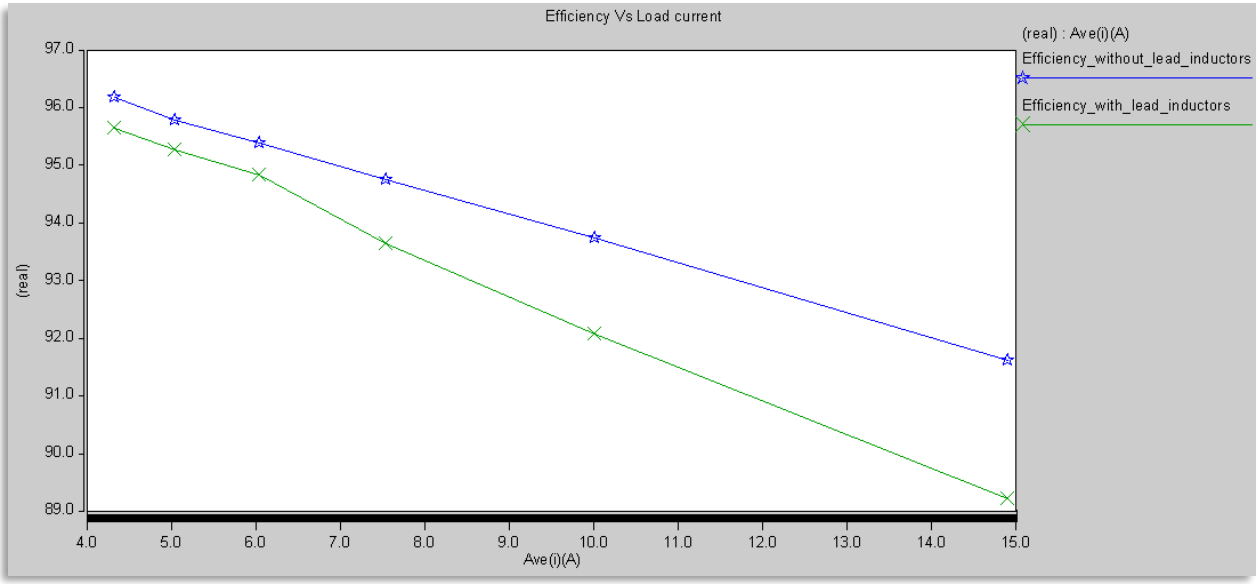


Figure 27: Results from exp2_efficiency_vs_load_current.ai_expt

3) UVLO operation

In experiment (*exp3_UVLO.ai_expt)*, the Under Voltage Lock Out condition is simulated by using Fault Analyzer. Fault Analyzer injects the required condition at VIN pin of UCC3882 by reducing the voltage to 9V and later increasing it to 12V. The System behavior when voltage falls below 10.5V and rises above 10V is studied in this experiment. Details of experiment with brief description of each section is given in Figure 28. And fault analysis settings are given in Figure 29.

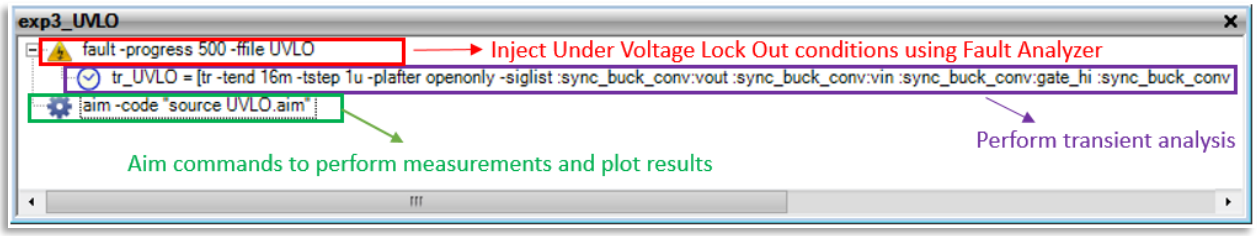


Figure 28: Experiment setup exp3_UVLO.ai_expt

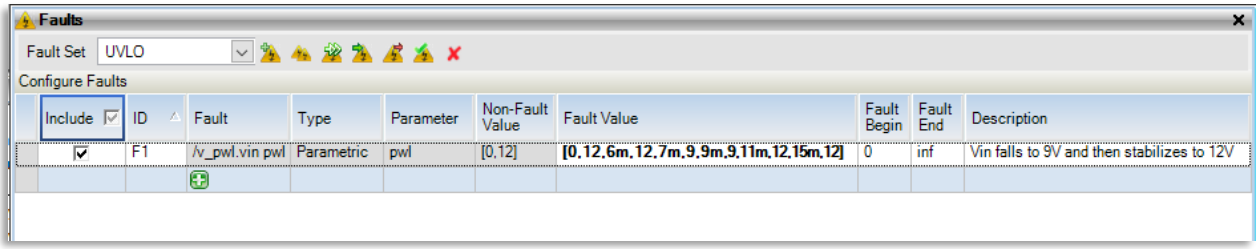


Figure 29: Fault settings for UVLO condition

After successful completion of simulation, waveforms are automatically loaded in graph using AIM codes as shown as Figure 30. It can see that when voltage at VIN pin drops below 10V, UVLO turn-on threshold is reached (with a hysteresis of 500mV) and the gate pulse to both High and Low side MOSFETs are stopped. Later, when the voltage rises above 10.5V, UVLO turn-off threshold is reached (with a hysteresis of 500mV) and the gate pulses are re-established to drive the MOSFETs.

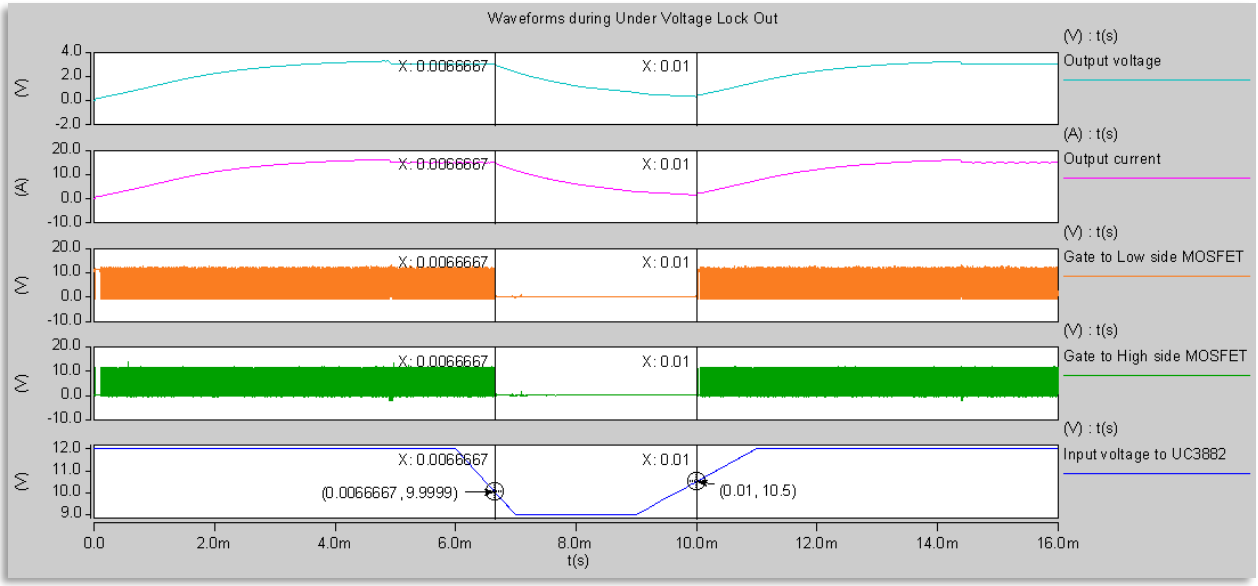


Figure 30: Results from exp3_UVLO.ai_expt

4) Six Sigma quality check

In experiment *exp4_six_sigma.ai_expt*, output voltage of the converter is verified for six sigma quality checks through 50 runs of Monte-Carlo (including extreme values). During the analysis, nominal value of resistors, ESR of capacitors and MOSFET parameters as specified in Tolerance ratings in Power MOSFET tool are varied. In each iteration of analysis, the variation in average value of output voltage after steady state is monitored. The maximum and minimum values of the variation is verified to check if the six sigma criteria are met. Details of experiment with brief description of each section is given in Figure 31.

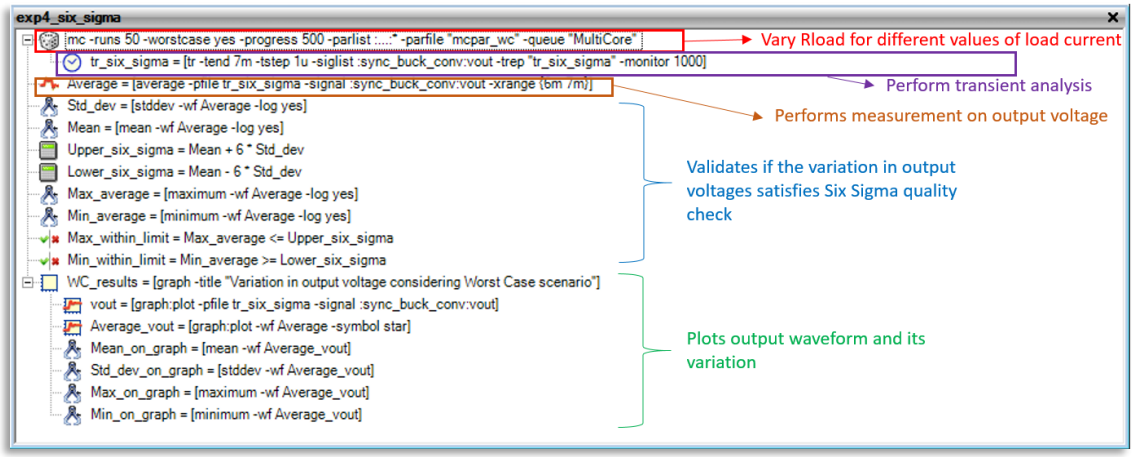
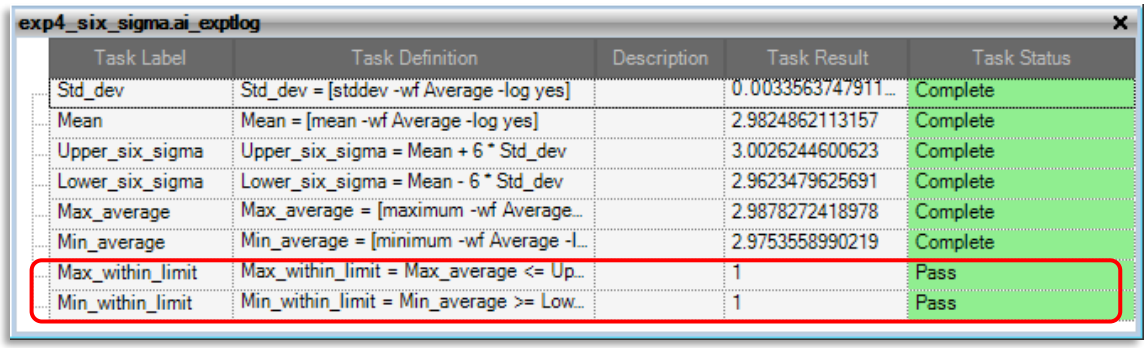


Figure 31: Experiment setup exp4_six_sigma.ai_expt

It will take some time to complete the simulation depending on the number of parallel runs explained earlier. After successful completion of simulation, the graphs are loaded in Results Tab. Open experiment report and it can be seen that the variation in output voltage is within six sigma criteria as shown in Figure 32.



exp4_six_sigma.ai_exptlog

Task Label	Task Definition	Description	Task Result	Task Status
Std_dev	Std_dev = [stddev -wf Average -log yes]		0.0033563747911...	Complete
Mean	Mean = [mean -wf Average -log yes]		2.9824862113157	Complete
Upper_six_sigma	Upper_six_sigma = Mean + 6 * Std_dev		3.0026244600623	Complete
Lower_six_sigma	Lower_six_sigma = Mean - 6 * Std_dev		2.9623479625691	Complete
Max_average	Max_average = [maximum -wf Average...		2.9878272418978	Complete
Min_average	Min_average = [minimum -wf Average -l...		2.9753558990219	Complete
Max_within_limit	Max_within_limit = Max_average <= Up...		1	Pass
Min_within_limit	Min_within_limit = Min_average >= Low...		1	Pass

Figure 32: Experiment report from exp4_six_sigma.ai_expt

Open graph “WC_results” from Results tab and output voltage waveform and variation of average value can be seen as shown in Figure 33.

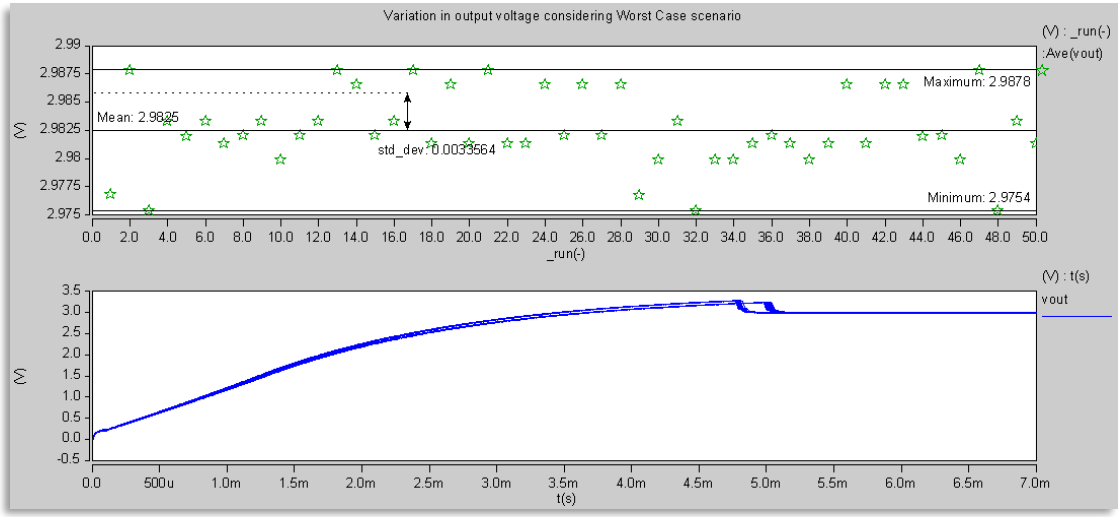


Figure 33: Results from exp4_six_sigma.ai_expt

Conclusion

The synchronous buck converter using UCC3882 is designed and simulated to study the normal operating condition and validated against design specifications. It was found that the lead inductors are causing more switching loss and reduced efficiency. Through simulation it is proven that by using improved packaging technique, the effect of lead inductors can be avoided and efficiency can be improved for Synchronous buck converter. System efficiency Vs load current was also simulated and found that this topology can be used in applications that demands very high efficiency. Operation during Under Voltage Lock Out (UVLO) were also carried out and found that UCC3882 has inbuilt protection circuit to monitor drop in supply voltage. Six Sigma quality check was also performed on the design and it was found that variation in output results met the criteria.

References

[1] http://www.ti.com/lit/ds/symlink/ucc3882-1.pdf

[2] Bo Wang, Rengang Chen, and David Jauregui, “Common source inductance (CSI) of power devices and the impacts on synchronous buck converters”, Applied Power Electronics Conference and Exposition (APEC), April 2014.

[3] http://www.ixys.com/Documents/AppNotes/IXAN0069.pdf

[4] http://www.ti.com/lit/an/slyt358/slyt358.pdf