



Chipset

South Bridge
eMMC: Unknown M52532 133ED255 (29.1 GB)

State After G3 [S0 State]

SCC eMMC Support [PCI mode]
SCC SDIO Support [ACPI Mode]
ISH Support (D10:F0) [Disabled]
LPE Audio Support [LPE Audio ACPI mode]
Onboard PCIe LAN [Enabled]
UART Interface Select [Enabled]

USB OTG Support [PCI mode]
Default DRD Config [HostMode]
DRD Access Method [Sideband]

LPSS Configuration
LPSS DMA #1 Support [ACPI Mode]
LPSS DMA #2 Support [ACPI Mode]

Specify what state to go to when power is re-applied after a power failure (G3 state)

- ←→: Select Screen
- ↑↓/Click: Select Item
- Enter/Db1 Click: Select
- +/-: Change Opt.
- F1: General Help
- F2: Previous Values
- F3: Optimized Defaults
- F4: Save & Exit
- ESC/Right Click: Exit